B 1700

96 COLUMN MFCU CONTROL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Burroughs

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INDEX

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Introduction and Operation

GENERAL DESCRIPTION

The MF-96 Card Control, controls any of a series of 96-column card handling equipment, with various operating speeds and various combinations of punch, print, read, and sort functions. Any of these units can be connected, with no modification or adjustment to the control. One peripheral unit may be connected. The peripheral units of this series have a common interface design. The control responds to a command from the processor in a manner independent of the type of device connected. For instance, the read function is performed similarly on the fast reader, slow reader, multifunction unit, or any unit capable of the read function. Operation at the control-peripheral interface is asynchronous, and therefore insensitive to the various operating speeds. However, certain variants of the OP-code must be appropriate for the unit connected, so the computer program must have information on which type device is installed. The result of fault or error conditions also varies between different types of units.

The control does not detect which type of device is connected, and therefore cannot protect against commands impossible for the connected device, (e.g. punch command on a card reader). The result in such a case is undefined, and the control may reach a state from which it can be removed only by clearing. The control also does not detect which cables are connected, and does not reject a command which would require a cable which is not connected.

Table I-1

INTERFACE

B NUMBER	DESCRIPTION
B-9419-1,2,4	Read, Punch, Print, Key Board with Interface
9119-1	Reader, 300 CPM
9119-2	Reader, 1000 CPM
9219-1	Punch, 60 CPM
9219-2	Punch-Print, 60/60 CPM
9219-3	Punch, 120 CPM
9219-4	Punch-Print, 120/120 CPM
9319-1	Read-Punch, 300/60 CPM
9319-2	Read-Punch-Print, 300/60/60 CPM
9319-3	Read-Punch, 500/120 CPM
9319-4	Read-Punch-Print, 500/120/120 CPM
9319-5	Multifunction Unit (Read-Punch-Print) 1000/500 120/120 CPM
PC 9101	Recorder (with off-line keypunch capability)
PC 9201	Recorder-Print (with off-line keypunch capability)
PC 9301	Recorder-Print-Sort (with off-line keypunch capability)

There are two possible cables from the control to the peripheral unit, one primarily for the read function, the other primarily for the punch-print function. Readers employ only the read cable; punch-print units employ only the punch-print cable; multifunction and read-punch-print units employ both cables. Signals required for all units, e.g. card motion signals, stacker select signals, etc., are available on both cables.

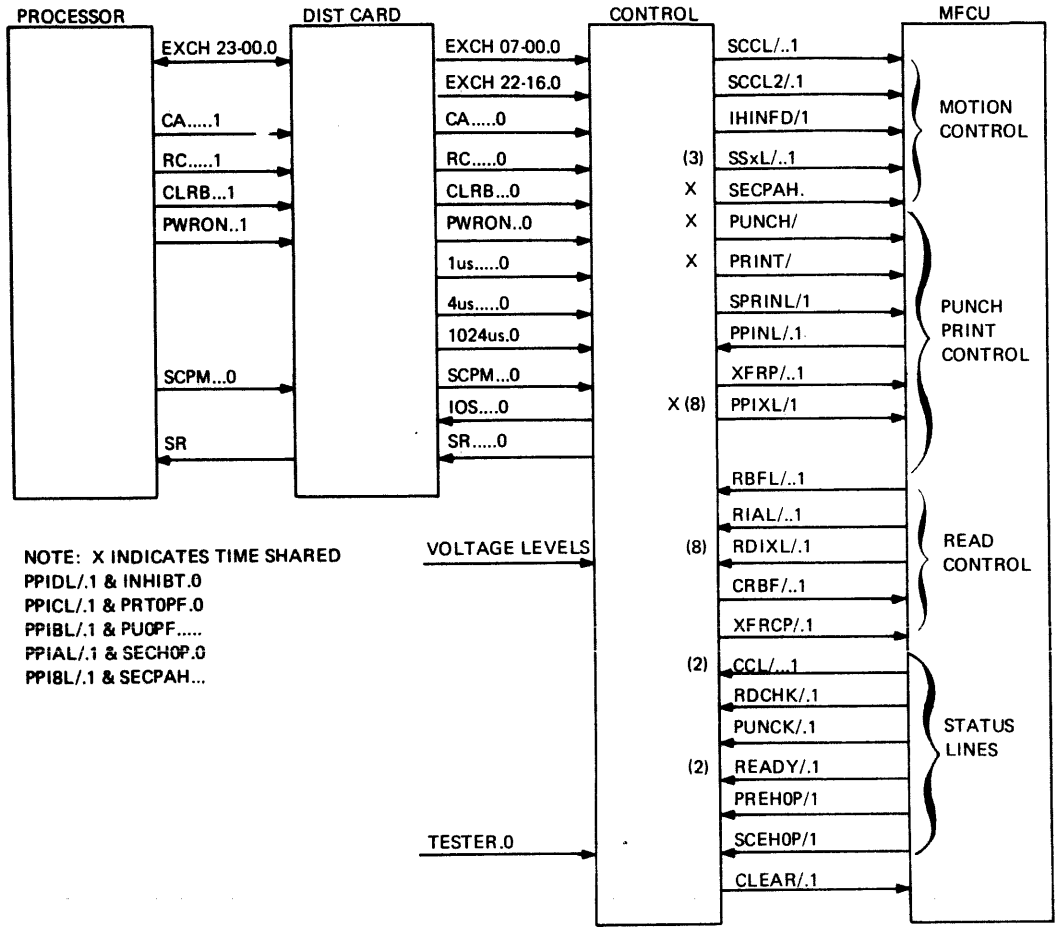
Figure I-1 illustrates the data & control lines which interface the Processor, Distribution Card & Subdistribution Card (if applicable) the Multi-Function Card Unit (MFCU), Control, and the MFCU Device. The numbers (8) within the Control Block indicate the number of levels the particular term to the right consists of. e.g. (8) RDIXL/.1 indicates RDI (D,C,B,A,8,4,2, & 1) L/.1. In addition to the primary use of interface lines between the Control and the MFCU, five of these lines are time shared with other signals. The five levels which are time shared are the PPIXL/.1 levels, D,C,B,A,&8 as shown.

TYPE OF CODE

The MFCU use an internal BCD Card Code. The Control provides translation from the internal BCD Card Code to an eight bit EBCDIC Code during read operations when specified in the I/O Descriptor. During Punch Operations, translation from EBCDIC to BCD can be specified. During print operations the 6 bit BCD code must be sent to the Printer.

DATA STORAGE

An 8 x 100 bit MOS Register provides storage within the control for 96 characters, of Punch, Print, or Read Data, plus three 8 bit bytes of the Reference Address. The MFCU Device also provides three separate buffers, each capable of storing 96 characters.



Sec. I-1 INTERFACE: (PROCESSOR/CONTROL/MFCU)

OPERATION

Character serial data is transferred to/from the Control and Processor under soft ware control. Character serial data is transferred to/from the MFCU and Control under the control of both the Control and device. Four basic operations are available, defined as follows:

(Punch/Print/Read Operation)

Punch Only, Print Only, or Read Only can be specified as well as any combination of the three operations. In addition, when Punch and Print is specified, the data may be either the same or different.

During all read operations, the control checks for a ? character in the first column, indicating a control card. The card is left in the wait station and no additional card is drawn from the hopper, as this may be the last card to be processed. The control transmits to the processor a Result Descriptor containing validity check.

Card throughput is reduced if the processor delays response to Service Request, particularly in the READ operation.

READ REPEAT OPERATION

Two types of read operation are provided to obtain optimum performance. The READ-REPEAT operation reads at maximum read speed for all readers. The operation cannot be performed in conjunction with punch, print, read, or stack select (i.e. stack select must be overflow mode).

The read operation used in conjunction with the PUNCH/PRINT/READ Operation is somewhat slower in operation. However, additional capabilities are provided, such as: Punching, Printing, and/or Stacker select.

READ-REPEAT is affected only by long delays (on the order to 50 milliseconds for a high speed reader), as card motion is concurrent with control-processor communication.

TEST OPERATION

A test operation is used when initiated by the Processor (under soft ware control) to determine the following:

1. MFCU Ready condition
2. Hopper 1 Empty
3. Hopper 2 Empty

PAUSE OPERATION

A pause operation is used when initiated by the Processor (under software control) to generate a pause of 1024 usec. The pause operation is used by software to allow time to service the controls last operation.

ERROR DETECTION

The peripheral unit checks for data errors, both read and punch, and upon detecting an error, takes initial corrective action without control intervention. The control receives signals indicating the type of error, and proceeds according to the type of error.

READ ERROR

Read operations are checked by the double-strobe technique (triple strobe for high speed units). Upon detection of read check, retains the read error card in the wait station, signals read check, and remains ready. The control returns to the processor a Result Descriptor indicating read check.

PUNCH ERROR

All punch units check the data punched by means of a post-punch read operation. Regardless of punch error detection, the card proceeds to the stackers at normal speed. The punch error is detected early enough to route the card to the error stacker. To avoid placing cards in the normal stacker out of correct sequence and to simplify the error recovery procedure, the following card, if it has reached the punch station, will be punched/printed, and placed in the error stacker. It will not be checked for punch error.

Any card in a wait station will remain in the wait station. The unit remains ready, signals the control that a punch check has occurred. The control then does not feed another card, and transmits to the processor a Result Descriptor indicating the punch check. The punch error report is delayed one cycle because the post-punch read station is some distance from the punch station, causing the punch error recovery procedure to be slightly more complex than that for a read check.

GLOSSARY OF TERMS

REGISTERS AND COUNTERS

Command Register	The command register accepts all commands to all channels when CA is true. The commands are sent on Exch lines 20 - 23.
Command Variant Register	Accepts all command variants to all channels when Exch line 20 is true and 21 & 22 are false, which indicates a Control Command. The command variants are set in the register when CA is true. The register is cleared when the Exch line 20 is false and the clock occurs. Exch line 20 designates a control command. Note that each control must accept all commands and command variants as the Test Service Request Command is sent to all channels with no channel number designated.
OP-Register	Accepts the first 8 bit byte of the I/O Descriptor at STC01, the second byte at STC02.
Input Register	Accepts 8-bit bytes of data from Exch lines 00-07. In addition, it accepts read data from the device via the Read Data Lines (RDIXL), either directly or through a BCL to EBCDIC Translator. The input register can also receive the 3 bytes of the reference address via the output register. All data to be shifted thru the 8 x 100 bit MOS Shift Register must first be set in the input register.

Output Register	The output register is the holding register for all data shifted out of the MOS shift register. The data in the output register can be gated to either the input register (to circulate the reference address, the Exch lines 00-07 or the Punch Print Information lines (PPIXL). Gating to the PPIXL lines can be either direct or through a EBCDIC to BCL Translator.
8 X 100 bit MOS Shift Register	100 bits in length and 8 bits high the register requires a two phase clock drive to complete a shift right by one of the entire 100 eight bit positions. Each shift right by one requires four system clock periods. The register is used to store Punch/Print/Read data plus the 3 bytes of the reference address in the control.
Status Counter	(STC) Keeps count of the status counts (00-23). The status count is returned to the processor during the RC portion of all commands except the Test Service Request request.
Byte Counter	(BCNT) Counts the number of Bytes (8 bits of data) in the MOS Register. The BCNT counter is incremented by 1 when a shift occurs during STC10
INTERFACE: (CONTROL/MFCU)	
SCCL (Cont to Dev)	Start Card Cycle Level will advance the card from the wait station through the Punch/Print Path to a selected stacker. The same SCCL will feed a card from a selected input hopper through the read station to the wait station. SCCL remains true until CCL goes true, or ready goes false.
IHINFD (C to D)	Inhibit Feed disables feeding a card from the selected Input Hopper. Its used to get the last card of a file out of the wait station.
SS XL (C to D)	Stacker Select Levels (4, 2 & 1) refer to I/O Descriptor Sec. II.
SEC PAH (C to D)	Secondary path indicates the card is fed from the secondary input hopper. When false, cards from the primary input hopper are fed, SECPAH is time shared with PPI8L
PUNCH (C to D)	Indicates the card passing through each punch station will be punched. PUNCH is time shared with PPIBL.
PRINT (C to D)	Indicates the card passing through the print station will be printed. PRINT is time shared with PPICL.
SPRINL (C to D)	Separate Print Information Level indicates when PUNCH and PRINT are true that the data printed will be different from the data punched. When SPRING is false the data punched is also printed when Punch and Print are true.
PPINL (D to C)	Punch Print Information Needed Level indicates the device is ready to accept a 6-bit punch or print character. PPINL goes true after SCCL goes true. PPINL will not go true when Read Buffer Full is true.
XFRP (C to D)	Transfer pulse when true will allow the Punch/Print information to be loaded into the Punch Buffer and PPINL will go false.
PPIXL (C to D)	Punch Print Information Levels X=(D,C,B,A,8,4,2,1). Six levels are used for BCL Data transfer to the device and are strobed with XFRP.
RBFL (D to C)	Read Buffer Full Level is true when the last column of information has been read from the card to the read buffer in the device. It goes false after the 96th XFRCP or after Clear Read Buffer goes true.
RIAL (D to C)	Read Information Available Level goes true when RBFL goes true and stays true until XFRCP goes true. It goes true again when XFRCP goes false and repeats the cycle until the read buffer is empty.
RDIXL (D to C)	Read information lines X=D,C,V,A,8,4,2,1. The read information is available on lines B,A,8,4,2,1 & 1 when RIAL is true. Lines D, C are not used at present.
CRBF (C to D)	Clear Read Buffer Full is used to terminate a transfer of the read data in the Devices Buffer to the Control. CRBF is sent instead of XFRCP when the read data is not desired. When pulsed true will clear Read Buffer Full and when held true will inhibit Read Buffer Full.
XFRCP (D to C)	Transfer clock pulse is used when unloading the Read Buffer to the Control. It indicates the Controlling System has taken the character on the RDIXL lines, and is ready for the next character.

CCL (D to C)

Card Cycle Level goes true in response to SCCL and indicates the Device is processing a card, and is therefore not available for a new SCCL. SCCL can go true when CCL is false. CCL implies ready.

RDCHK (D to C)

Read Check goes true during card cycle level (CCL) for one of three possible conditions:

A. Light Check:

If any of the read station outputs (including amplifiers and other related circuitry) indicate a dark condition at the beginning of an input feed, read check will go true.

B. Dark Check:

If any of the read station outputs (including amplifiers and other related circuitry) indicate a light condition when the leading edge of the card is covering the read station, read check will go true.

C. Strobe Check:

As each card passes through the read station, the column information is strobed two/three times. See appropriate peripheral information for precise definition. The binary state of the information as interpreted by the respective strobing systems is defined by the following truth table.

DOUBLE STROBE

ZERO	ONE	READ CHECK
00	11	01
		10

TRIPLE STROBE

ZERO	ONE	READ CHECK
000	111	100
	011	001
	110	101
		010

Option 1/Option 2 is an installation selectable mode of operation which effects read check performance as follows:

Option 1. read check will cause ready to go false.

Option 2. read check will not effect ready. Read check will be reset by error recovery procedure.

PUNCK (D to C)

Punch errors are detected by a post-punch read station beyond the punch station. Punch errors are indicated after the following cards have entered the punch station and punching has started. The following conditions determine reaction to the punch error:

1. Error card will be routed to error stacker unless operator has set out-sort switch to non-out-sort mode.

2. Card in punch process will be completed and routed to same pocket as error card.
Units which do not have readers will indicate punch error on every card if

pre-punched cards are inputed. One end card is required at the end of each deck to maintain ready until the controlling system can detect and evaluate the error condition.

The Option 1/Option 2 feature is an installation selectable mode of operation which effects punch error performance as follows:

Option 1, punch error will cause ready to go false.

Option 2, punch error will not effect ready. Punch error will be reset by the error recovery procedure shown in note 1 of section 3.4.

Note 1:

Error recovery procedure
The system will keep a record of all cards being read, punched and printed.

When on-line, punch/read errors can only be reset by SCCL or system clear.

(1) Read check to be defined.

READY (D to C) Ready is false when any of the following conditions have been detected:

A. Power off
B. System clear
C. Interlocks open
D. On-line switch is off
E. Full stacker
F. Input check
G. Output check
H. Stop/reset switch pressed
I. Punch check (option 1 mode)
J. All feed hoppers and wait stations empty
K. Read check (option 1 mode)

PREHOP (D to C) Primary hopper empty is true if there are no cards in the primary hopper.

SCEHOP (D to C) Secondary hopper empty is true if there are no cards in the secondary hopper.

CLEAR (C to D) Clear when true makes the device not ready. It clears the overflow mode, clears error logic if error conditions are corrected, and resets commands when ON-Line.

CONTROL MNEMONICS

BUS OC	Operation completed to BUS.
CLRF	Clear F.F.
CLTS	Clear and Test Status
CLRRDBF	Clear Read Buffer Full
CMR	Command Register
CIRCF	Circulate F.F.
CCLF	Card Cycle F.F.
CRBFF	Clear Read Buffer (in divice)
CONV	Control Variant Register
CODE6	Data Transplated
DEV-DEP	Device Dependent
DP	Device Present
EXCEPT	Exception Bit in R/D
FEEDF	Feed F.F.
INHFDF	Inhibit Feed F.F.
INCSHF	Increment Shift
IR/OR	Input Register or Output Register
ID C	Channel ID (Channel #)
INVALF	Invalid F.F.
LOADF	Load F.F.
LOOPF	Loop F.F.
OPSTF	Operation Started
OPCOMP	Operation Completed
PRIMF	Primary Hopper F.F.

PUDONEF	Punch Done F.F.
PHE	Primary Hopper Empty
PUNCK	Punch Check Level
PUOPF	Punch OP F.F.
PRTOPF	Printer OP F.F.
PPINL	Punch Printer Info Needed Level
PPIXL	Punch Printer Transfer Level
PREHOP	Primary Hopper Empty (R/D)
RBFF	Reader Buffer Full F.F.
RDCK	Read Check Level
RDOPF	Reader OP F.F.
READYF	Ready F.F.
SECF	Secondary Hopper F.F.
SECHOP	Secondary Hopper
SHE	Secondary Hopper Empty
SCCLF	Start Card Cycle F.F.
STC	Status Counter
SERSK	Service Request Mask
SPRF	Service Request F.F.
SPRINL	Separate Printer Info Level
SECEHOP	Secondary Hopper Empty (R/D)
TSTA	Test Status
UNLOADF	Unload F.F.
XFRCP	Transfer Clock Pulse
XFROTA	Transfer Out Fase A (out of processor)
XFROTB	Transfer Out Fase B (out of processor)
XFROTAD	Transfer Out Fase A Direct (out of processor)
XFERIN	Transfer In (to processor)
CKOP	Check OP Code
ID BUS	ID# to BUS

Functional Detail

I/O DESCRIPTOR

The Multi Function Card Unit (MFCU) is capable of executing any of four I/O Descriptors (also referred to as OP-Codes). Each Descriptor is 24-bits in length. The bit positions of the Descriptors indicated by a period (.) have no significance and should be set to zero.

PUNCH/PRINT/READ OP

The Punch/Print/Read Op when received in the Control will cause a punch, print, read or any combination of the three operations to occur. 96 characters of information are always processed. The variable bits of the OP-Code (1 or 0) will designate the specific operation which is to be performed.

PUNCH/PRINT/READ OP

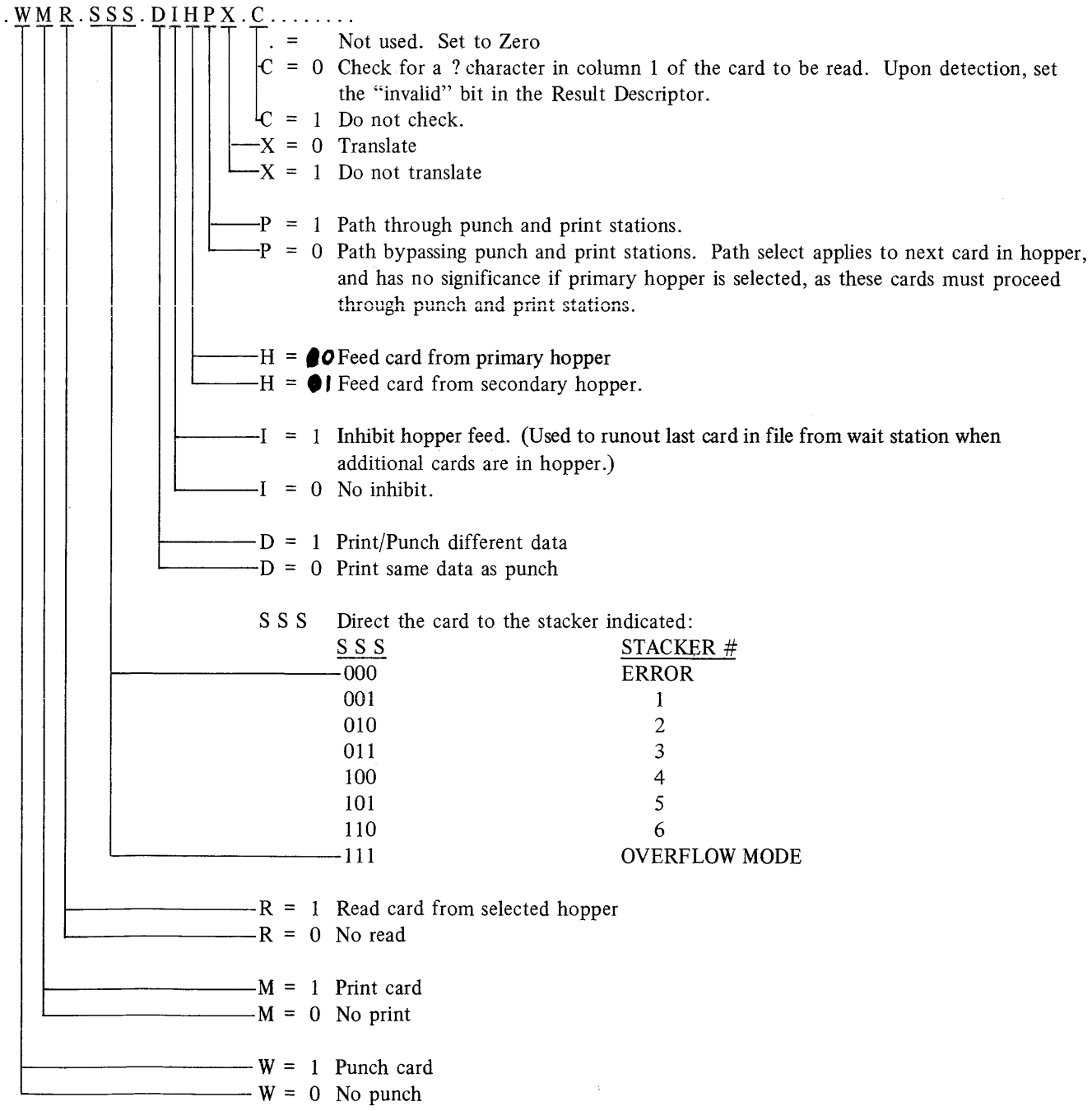


Fig. II-1

READ-REPEAT

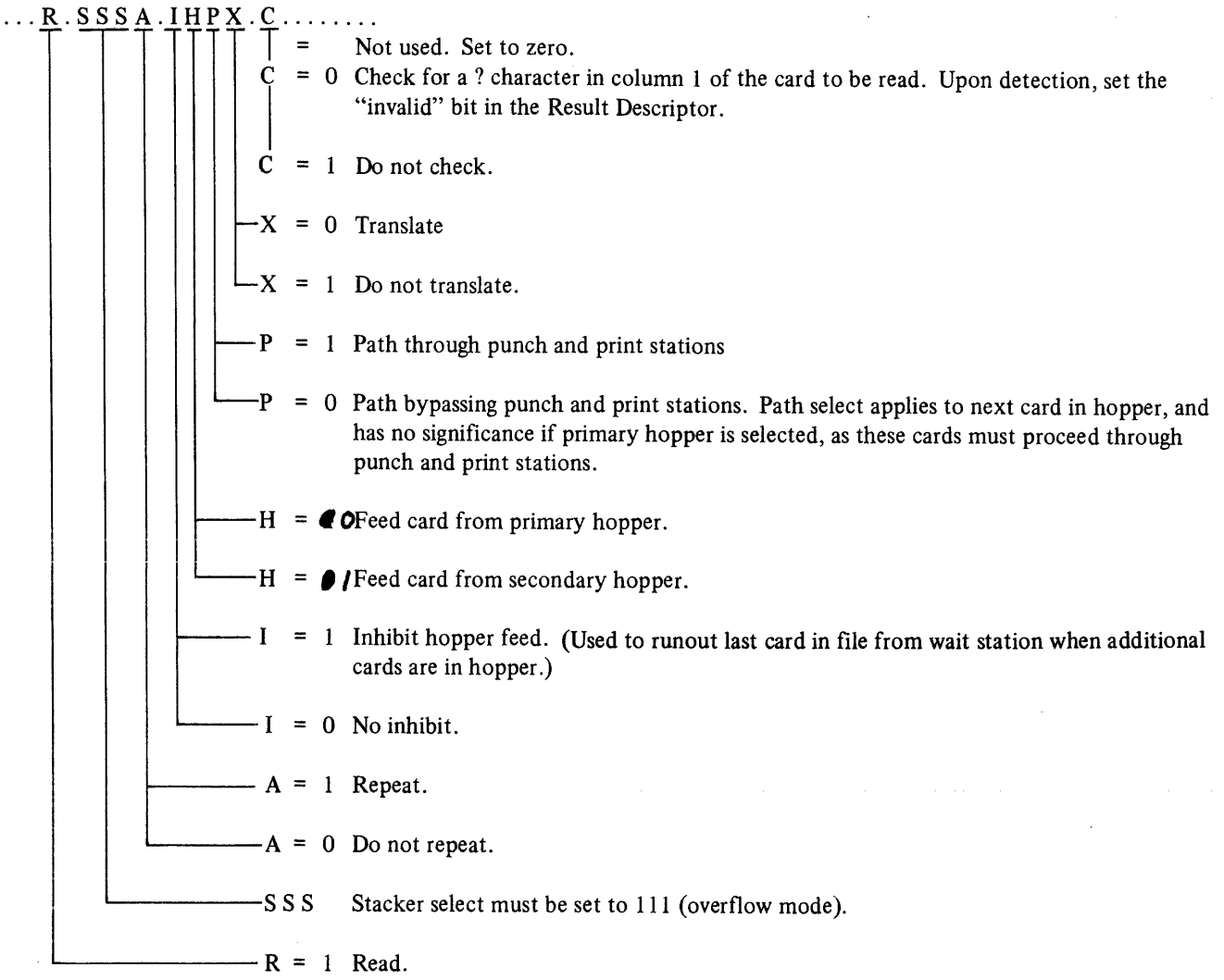


Fig. II-2

With card in wait station. Transfer the read data from the card in the wait station to the processor. Transfer the card to the stacker. Feed and read the next card, leaving the card in the wait station, and storing the data.

With no card in wait station. Feed and read a card from the selected hopper, transfer the data to the processor, and transfer the card to the stacker. Feed and read the next card, leaving the card in the wait station and storing the data.

TEST

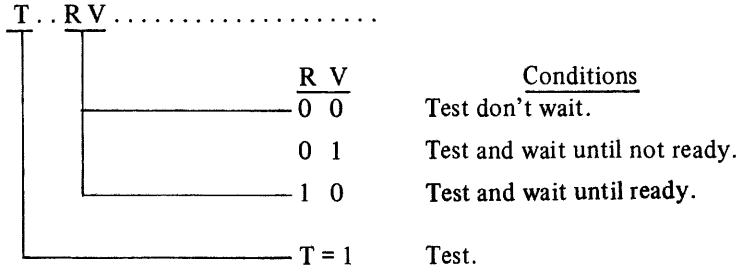


Fig. II-3

Test the unit for the following conditions:

1. Not Ready
2. Hopper 1 Empty
3. Hopper 2 Empty

In addition, the ID bits are returned during test.

PAUSE

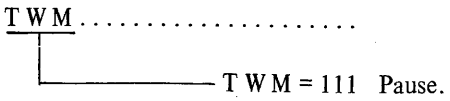
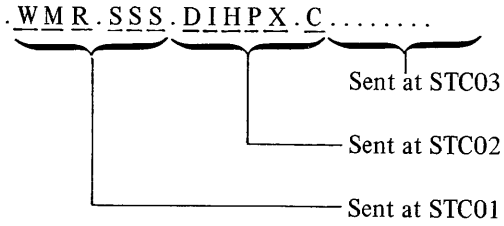


Fig. II-4

The Pause OP will return a Service Request after a pause of 8 milliseconds. The result descriptor returned must not have the operation complete bit set. This OP-code is sent to the control by the I/O interpreter program when the next I/O descriptor is not yet available for execution. Upon completion of any pause, the next I/O descriptor is inspected by the I/O interpreter program to see if it is ready for execution.

I/O DESCRIPTOR TRANSFER TIMES

The 24 Bit I/O Descriptor is sent to the Control in three 8-Bit Bytes. The first byte is sent as State Count 01 time (STC01), the second at STC02, and the third at STC03. The first byte sent as STC01 time will always contain bits of the I/O Descriptor. The second byte will contain bits of the I/O Descriptor only when either Punch/Print/Read or Read-Repeat. The third byte will always contain zeros which have no significance to the control. Refer to the example of the Punch/Print/Read OP transfer times illustrated in Figure II-



Punch/Print/Read OP, I/O Descriptor
Transfer Times

Fig. II-5

RESULT INFORMATION

At the completion of executing any of the four I/O Descriptors, a 24-Bit Result Descriptor is available. The Processor (under software control) must transfer the result descriptor from the Control to the Processor. The information available in the 24-Bit Result Descriptor is as follows:

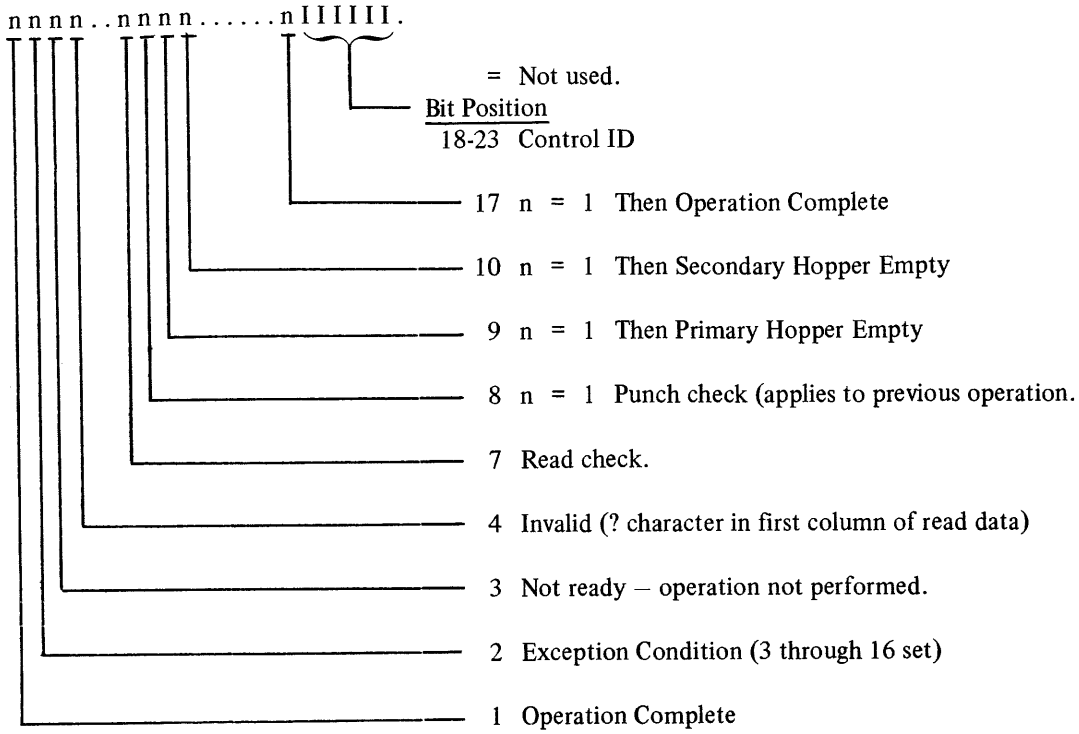


Fig. II-6 RESULT INFORMATION

Not ready is caused by any of the following:

Power off
System Clear
Interlocks open
On-line switch off
Full stacker
Feed check (card failed to reach read station, not advancing properly)
Stop/Reset switch actuated
All hoppers and wait stations empty
Output check (card beyond read station not advancing properly)

If the control receives an operation which includes a feed from an empty hopper, no card is moved, and the Result Descriptor is sent, indicating the empty hopper. The unit remains ready.

During all operations except PAUSE-op and TEST-op, empty hopper is indicated in the Result Descriptor only if the operation included feeding a card from an empty hopper. Empty hopper is not indicated on the operation that removes the last card from the hopper. If the other hopper is empty, it will not be indicated. During PAUSE or TEST operations, empty hoppers are indicated.

If the control receives an operation to punch or print a card from an empty wait station, the device moves no card and goes not ready. The control transmits the Result Descriptor with Ready bit false.

RESULT INFORMATION TRANSFER TIMES

The 24-bit result information available is sent to the Processor from the Control in three 8-Bit Bytes. The first Byte is sent at STC21, the second at STC22, and the third at STC23. Refer to Figure II-7 which illustrates a MFCU result Descriptor showing OP-Complete and Read Check.

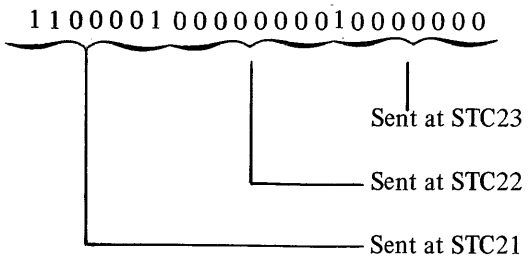


Fig. II-7 RESULT INFORMATION TRANSFER TIMES

DATA TRANSFER (PROCESSOR/CONTROL/MFCU)

Figure II-8, Block Diagram of Data Transfer, illustrates the Data flow paths within the Control. In addition, the transfer path in/from the Process via the Exchange lines is shown and the transfer path for Punch, Print & Read Data to/from the MFCU via either the Read Information lines or the Punch/Print Information lines. Translation of Read Data from BCL to EBCDIC can be specified as well as translation from EBCDIC to BCL for Punch or Print Data. All data to and from the 8 X 100 Bit MOS Register must be set in the Input Register and Output Register, respectfully.

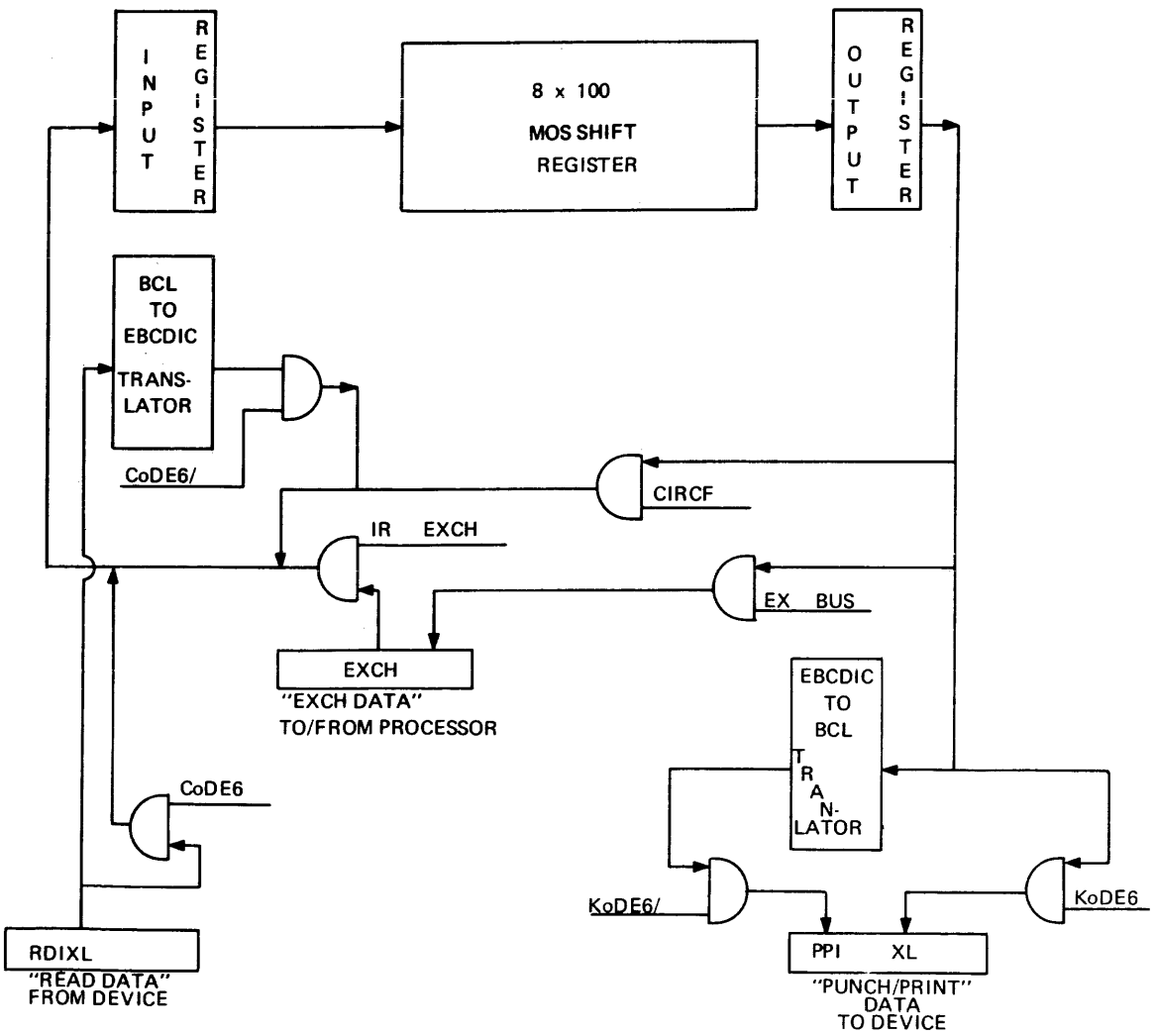


Fig. II-8 DATA TRANSFER (PROCESSOR/CONTROL/MFCU) BLOCK DIAGRAM

DATA TRANSFER (MOS REGISTER)

Each of the OP - Codes available will cause certain data to shift through the MOS Register in a particular sequence. The following figures illustrate the position of either Punch Print and/or Read Data, and the Reference Address in the MOS shift register at the various status counts. A zero (-0-) indicates zero bits are shifted into the register. The 3, 2, and 1s indicate the 3rd, 2nd and 1st bytes of the reference address. Data is specified as either Punch and/or Print or Read Data.

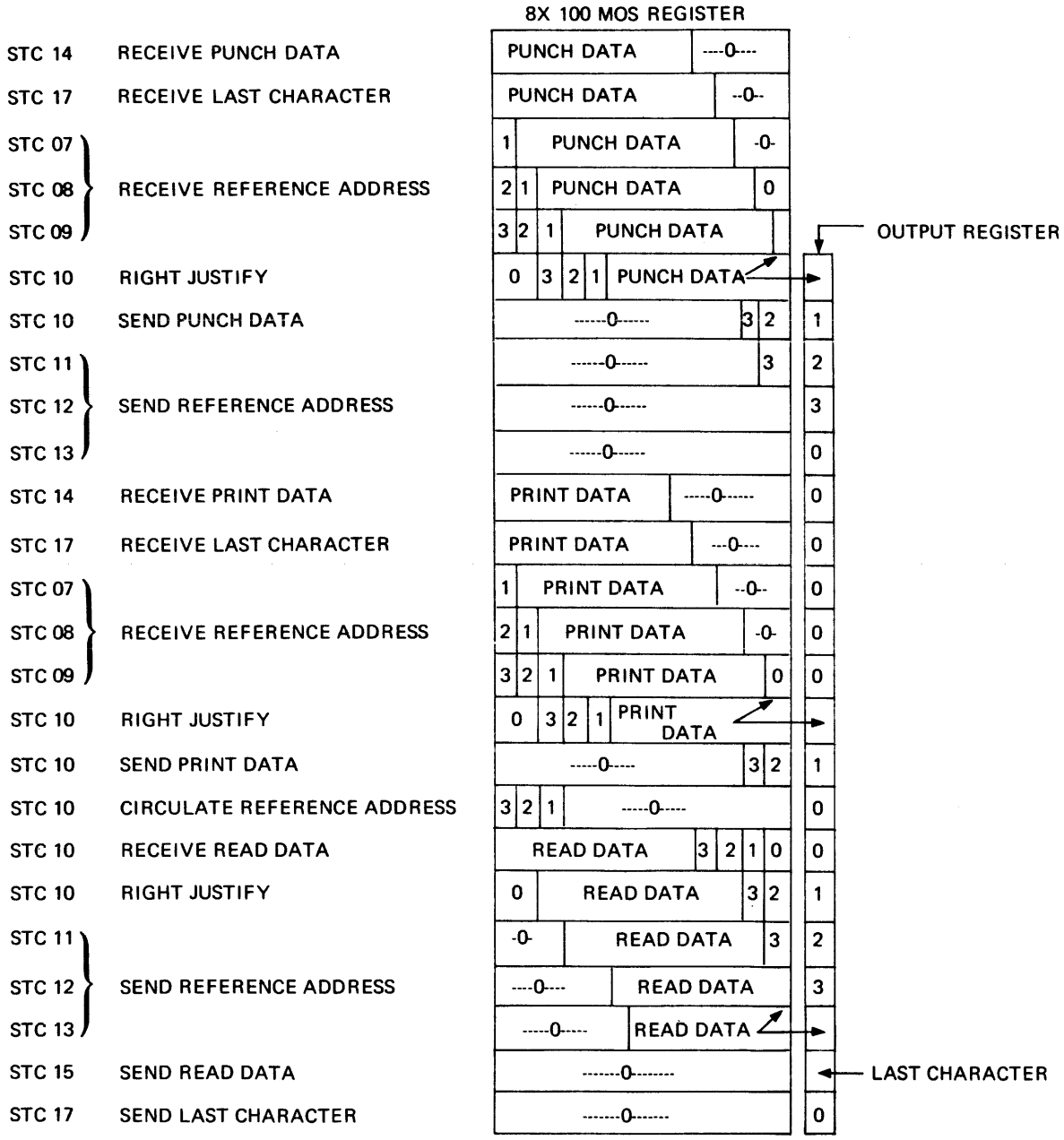


Fig. II-9 PUNCH/PRINT/READ & DIFF
DATA TRANSFER

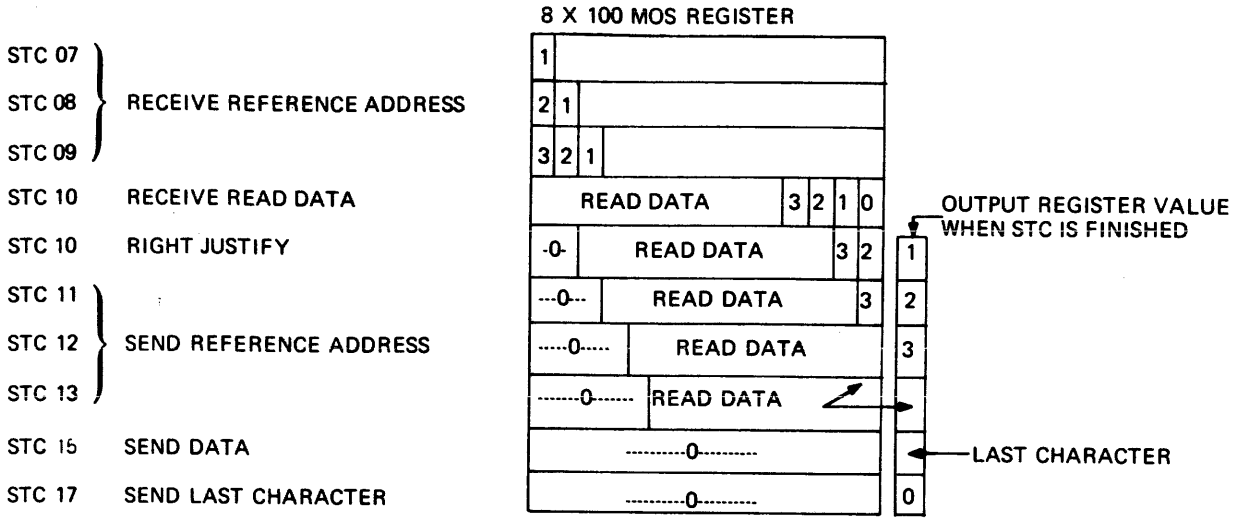


Fig. II-10 READ OP ONLY DATA TRANSFER

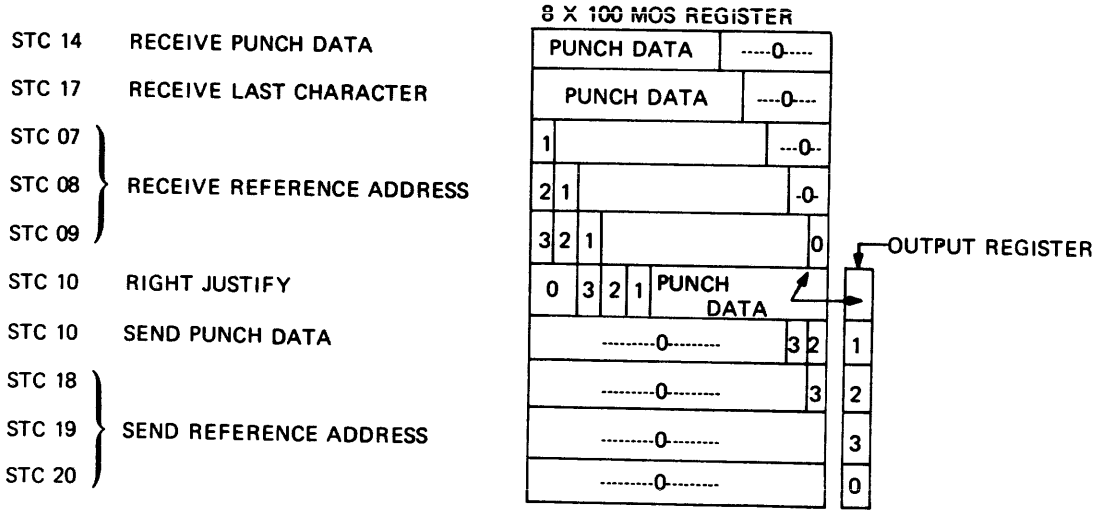


Fig. II-11 PUNCH OP OR PRINT OP DATA TRANSFER

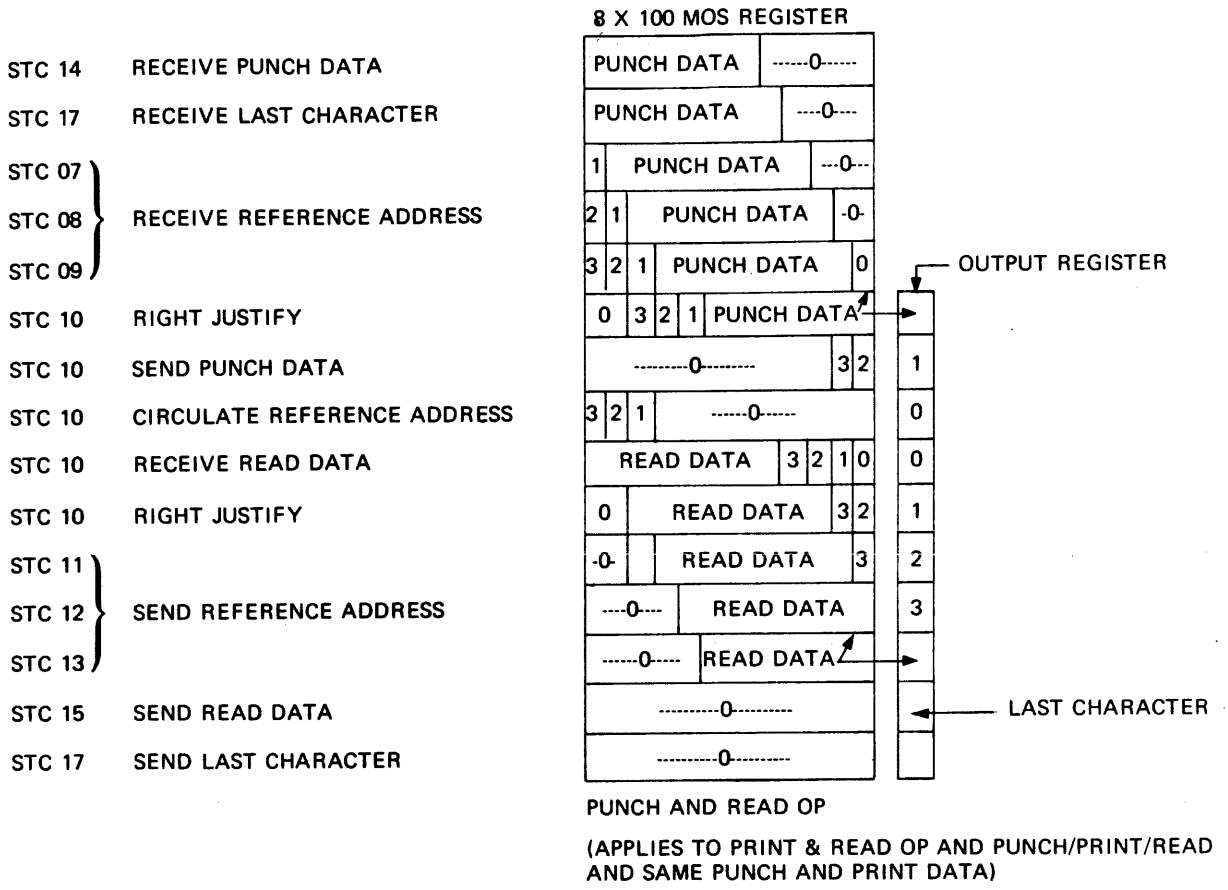


Fig. II-12 DATA TRANSFER

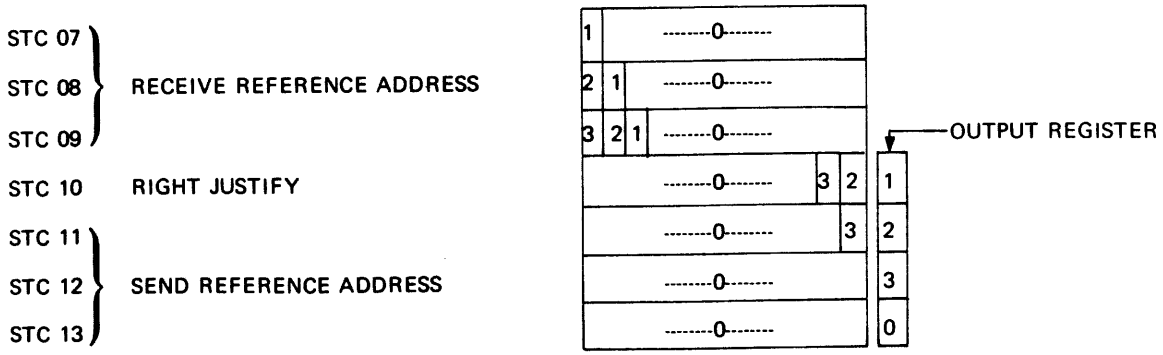


Fig. II-13 TEST OR PAUSE OP DATA TRANSFER

Read OP "Only"

STC	Action	Line #	Action		
1	Receive				
2	Op-Code				
3					
4					
5					
6					
7	Receive				
8	Reference				
9	Address				
10	----------	1	SCCLF←1	Start Card Cycle Level	"Feed Card from Input Hopper"
		65	RBFF←1	Read Buffer Full	"Set Flip-Flop"
		61	LOADF←1	Enable transferring Read Buffer to Control Buffer	
		67	RIALF←1	One character available from Device	
		68	PH2DY←1	Start Shift of MOS Register	
		69	XFRCP←1	Transfer Clock Pulse	
		70 or 71	Translate or Translate Not		
		85	LOADF←0	BCNT = 96	"One Card read to Control"
		86	INCSHF←1	BCNT = 96	
		22	PH2DY←1	Shift Reference Address (Byte 1) to output of MOS Register	
		24	OR←BUF	BCNT = 97 "Gate output of MOS to Output Register"	
		26	STC+1	Exit to STC 11	
		27	SRF←1	Set the Service Request Flip-Flop	
11	Send				
12	Reference				
13	Address				
15	Send Read Data in MOS Register to Processor				
17	Send Last Read Data "Character" in MOS to Processor				
21	Send				
22	Result				
23	Descriptor				
01					

Fig. II-14

SIMPLIFIED FLOWS:

PUNCH OP "PRINT OP IS SIMILAR"

STC	Action		
1	Receive OP-Code		
2			
3			
4			
5			
6	Determine OP-Code		
14	Receive Punch Data		
17	Receive Last Character of Punch Data (BCNT = 96)		
7	Receive Reference Address		
8			
9	(Set FEEDF)		
10	Line #	Action (Key actions only. Other Line Numbers & Actions occur.)	
	1	SCCLF←1	Start Card Cycle Level "Feed Card".
	18	INCSHF←1	
	25	UNLOADF←1	Gate OR to PPIXL (BCNT to oo)
	31	PPINLF←1	"PPINL from Device and UNLOADF"
	32	XFRCP←1	
	33	BUS←OR	
	34	PPIXL←BUS	Gate Output Register to Data Lines
	43	CRBFF←1	When BCNT again = 96
	49	BCNT←00	BCNT96 "Data all out to Punch Buffer"
	50	UNLOADF←0	
	67	RIALF←1	One Character of Read Data available
	72	CLRF←1	Clear Read Buffer
	79	LOADF←0	Reset Load
	80	STC+ 8	Exit to STC 18
	81	SRF←1	Ser Service Request Flip-Flop

	Action
18	Send Reference Address to Processor
19	
20	
21	Send Result Descriptor Byte 1
22	Send Result Descriptor Byte 2
23	Send Result Descriptor Byte 3

01

Fig. II-15

PUNCH-READ OP

STC	Action
1	--- Receive OP-Code Byte 1
2	--- Receive OP-Code Byte 2
3	--- Receive OP-Code Byte 3
4	
5	
6	Determine OP
14	Receive Punch Data
17	Receive Last Character of Punch Data
07	Receive Ref. Address Byte 1
08	Receive Ref. Address Byte 2
09	Receive Ref. Address Byte 3 and set FEEDF
10	Line #
	11 SCCLF←1
	18 INCSHF←1
	25 UNLOADF←1
	Punch Data to Punch Buffer
	40 CIRCF←1
	49 BCNT←0
	50 UNLOADF←0
	52 OR←BUF
	53 IR←OR
	54 PH2DY←1
	56
	Clean Up
	59 PUDONFF←1
	60 LOADF←1
	86 INCSHF←1
	22 PH2DY←1
	24 OR←BUF
	26 STC←1
	27 SRF←1
11	
12	Send Ref. Address
13	
15	Send Read Data
17	Send Last Character
21	
22	Send Result Descriptor
23	

Fig. II-16

Simplified Flow:

Punch/Print/Read & DIFF

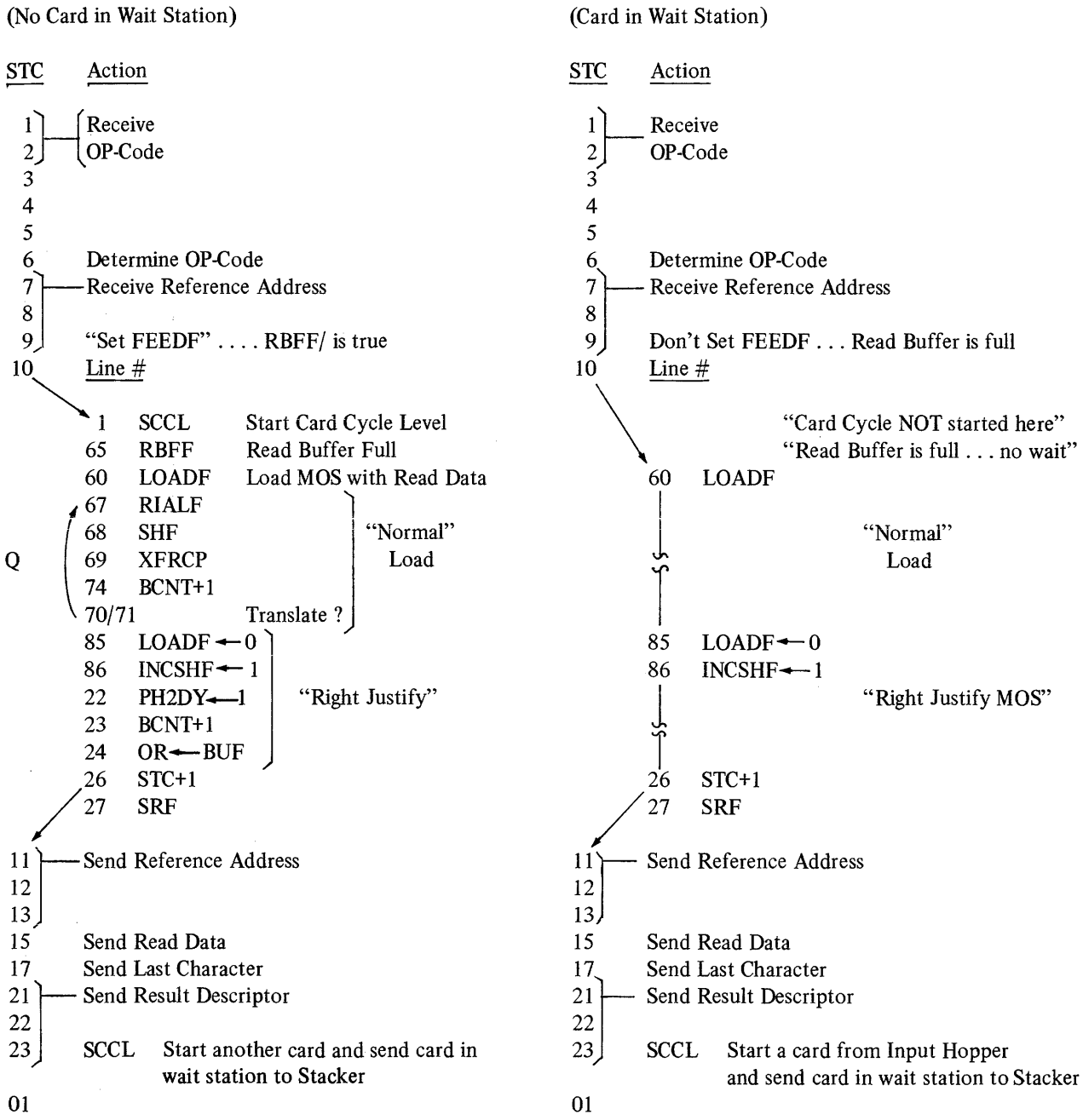
STC	Action
1	Receive OP-Code
2	
3	
4	
5	
6	Determine OP-Code
14	Receive Punch Data
17	Receive last character of Punch Data
7	Receive Reference Address
8	
9	
10	Line #
	1 SCCL Start Card Cycle Level
	18 INCSHF
	25 UNLOADF Gate OR to PPIXL
	↓↓ Punch Data to Punch Buffer
	47 STC+1
	48 SRF
11	Send Reference Address
12	
13	
14	Receive Print Data
17	Receive last character of Print Data
7	Receive Reference Address
8	
9	(Don't set FEEDF)
10	→ 10

STC	Line #	
	25	UNLOADF
	↓↓	Print Data To Print Buffer
	40	CIRCF Recirculate the Reference Address
	52	OR ← BUF
	53	IR ← OR
	54	SMF ← 1
	56	LOOPF ← 0
	57	CIRCF ← 0
	58	BCNT ← 00
	59	PUDONEF ← 1
	60	LOADF ← 1
	67	RIALF ← 1
	↓↓	Normal Load of Read Data from Device to MOS
	85	LOADF ← 0
	86	INCSHF ← 1
	22	PH2DY ← 1
	23	BONT+1
	26	STC+1
	27	SRF
11		Send Reference Address
12		
13		
15		Send Read Data to Processor
17		Send last character of Read Data
21		Send Result Descriptor
22		
23		
01		

Fig. II-17

READ REPEAT

READ-REPEAT OP "ONLY"



NOTE: Card started at STC23 with SCCL is read and read data is stored in Device Read Buffer.

Fig. II-18

TEST OP OR PAUSE OP

STC	Action
1	Receive OP-Code Byte 1
2	Receive OP-Code Byte 2
3	Receive OP-Code Byte 3
4	Dummy Count
5	Dummy Count
6	Determine OP-Code and Dummy Count
7	Receive Reference Address Byte 1
8	Receive Reference Address Byte 2
9	Receive Reference Address Byte 3
10	

Line #	Action
20	INCSHF←1 Right justify reference address after 8 milli second pause if pause OP Right justify reference address if test conditions are true

11	Send Reference Address Byte 1
12	Send Reference Address Byte 2
13	Send Reference Address Byte 3
21	Send Result Descriptor Byte 1
22	Send Result Descriptor Byte 2
23	Send Result Descriptor Byte 3

Fig. II-19

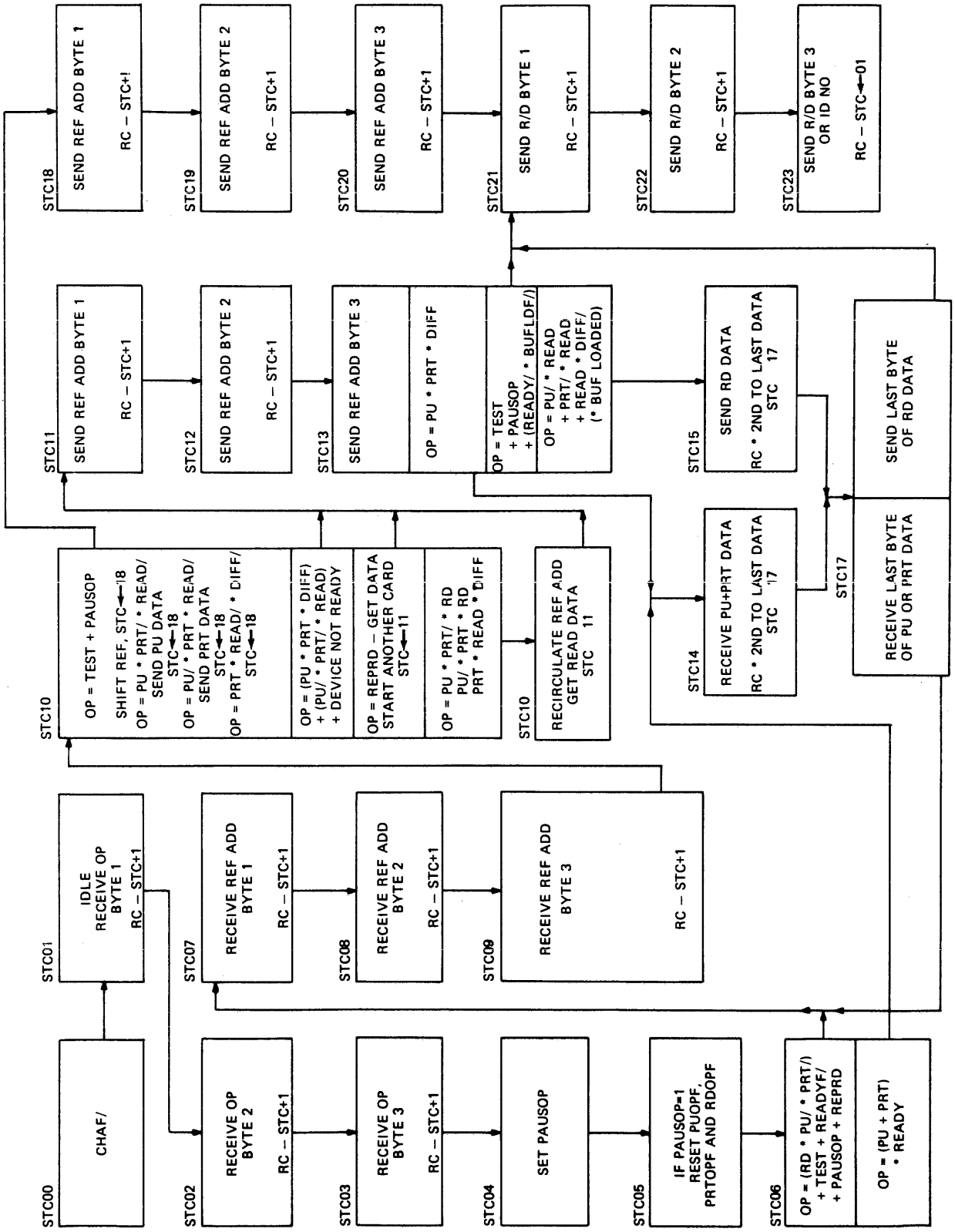


Fig. II-20 STATE DIAGRAM 96 COL. CARD CONTROL

96 COLUMN MFCU CONTROL DETAILED FLOW

STC = ANY	
CONV ← EX	CA*EXCH20* EXCH21/*EXCH22/
CMR ← EX CHAF ← 1	CA*CH
IR ← EXCH	CA*CH*XFROTAD
EXCH ← STC	CHAF*XFROTB/*TSR/
BUS ← ID BUS ← DP EX ← BUS	CHAF*(TSTA+CLTS)
IOS ← 1	CHAF + (TSR * CA/)
EX← SERSK	TSR*SRF
BCNT← 00 SRF ← 0 INHFDF ← 0 PUOPF ← 0 PRTOPF ← 0 PDOPF ← 0 LOOPF ← 0 INVALF ← 0 PUNCKF ← 0 RDCKF ← 0 PRIMF ← 0 SECF ← 0 OPREG ← 0 PUDONEF ← 0	RC*CHAF*CLTS

When CA is true and the command present on the Exchange is the Control Command, the command is set in the Command Variant Register. Note that a Test Service Request command does not designate a particular channel.

When CA is received and if the command present is designated for this Control, the Exch bits 22 thru 20 are set in the Command Register. CH true indicates the channel number sent with the command on EXCH lines 19 thru 16 compares to the channel number on this Control.
Set the Channel Active Flip-Flop (CHAF).

If the command received is Transfer Out A type then the EXCH lines 00 thru 07 are gated to the Input Register.

If the command received is not a Transfer Out B type and not a Test Service Request, the Status Count of the Control is gated to EXCH lines 20 thru 16. Note that with CHAF true, it indicates this is the phase B portion of a two phase cycle and this Control is designated.

If the command received is either Test Status or Clear and Test Status, the Channel ID bits are gated to the EXCH via the BUS. The Control ID is 011110 and is gated to the EXCH lines 06 thru 01 respectively. The Device Present bit is gated to the EXCH line 07.

If the command received is Test Service Request, then enable sending data to the Processor during the phase B portion of the TSR cycle. Note that TSR is true during the second phase of a command. If the command received is designated specifically for this Control, then CHAF is set and during the phase B portion of the cycle, IOS will enable sending data to the Processor.

If the command received is Test Service Request and the Control requires service by the Processor (indicated by the Service Request Flip-Flop set), the Service Request Mask is gated to the EXCH lines 00 thru 15. Note that only one of these lines will be enabled . . . that which designates the Control.

If the command received is the Clear & Test Status command, when RC is true, a general clear of Registers and Flip-Flops occurs.

CONTINUED ON NEXT PAGE

From STC = ANY

CHAF ← 0	RC
CONV ← 0	RC * CONTV/
READYF ← 0	READY/

When RC is true it indicates the phase B portion of a cycle is complete. CHAF is reset (if set) and the command variant register is reset (if set).

Reset the Ready Flip-FLOP is Not Ready.

The following four Flow boxes indicate the logic which occurs when a shift of the 100 byte MOS Register occurs. The logic can occur at STC = 07, 08, 09, 10, 11, 12, 13, 14, 15, 17, 18, and/or 19.

MOS	SHIFT LOGIC
PH2DY ← 1 CTL-PH2←0	SHF
CTL-PH1 ← 1 PH2DY ← 0	PH2DY
PH1DY ← 1 CTL-PH1 ← 0	CTL-PH1
CTL-PH2 ← 1 PH1DY ← 0	PH1DY

Quiescently CTL-PH2 is true. The DSCP pulse (trailing edge) which finds the Shift Pulse (SHF) true, will cause the phase delay register to set via the D-Set Mode; thus PH2 is set and all others are reset. Note that only CTL-PH2 is quiescently set "due to CLR initially"

PH2DY true, enables the shift up mode of the phase delay register. The next clock (trailing edge) will cause CTL-PH1 to set and PH2DY to reset.

The next clock also shifts the register up causing PH1DY to set and CTL-PH1 to reset.

The next clock shifts the register up causing CTL-PH2 to set and PH1DY to reset. After the clock occurs, the register is in the Bit Set mode as neither PH2DY, CTL-PH1, nor PH1DY are true. As soon as the next SHF is received, the register is in the D-Set Mode and the cycle repeats.

Note that CTL-PH1 and CTL-PH2 are inputs to the CTL to MOS Interface logic which generates the shift timing pulses of the MOS Register. The four outputs are also used as general enabling levels to sequence various functions.

STC00	
STC ← 01	CHAF/

Idle state of the Status Counter is STC01. The Control remains at STC01 until a Transfer Out command is received which designates this Control as the channel to receive the command.

STC01	
OPREG←EX	CA*CH*XFROTAD
READYF←1	READY

CH indicates the Transfer Out command received is for this channel. CH is true when the channel number compares with the channel number sent on Exchange lines 19 thru 16 from the Processor during the phase A portion of a Transfer Out command. The OP-Code is also sent on Exchange lines 07 thru 00. Note that only Byte 1 of the OP-Code is received which includes the 8 MSB of the I/O Descriptor or OP-Code.
Set the Ready FF if the device is ready.

CONTINUED ON NEXT PAGE

From STC = 01

STC+1	RC*CHAF*XFROTA	When RC is true, the Status Counter is incremented by 1. This is effectively the phase B portion of the Transfer Out command received for this channel.
WNOTRF←1	CA * CH ** FROTAD*EX03	
STC02		Receive Byte 2 of the OP-Code.
OPREG←EX	CA*CH*XFROTAD	The Exchange lines 07 thru 00 contain the next 8 MSB of the OP-Code. This includes the OP-Code variants D, I, H, P, X, & C if the OP-Code (MSB) received at STC01 is either READ, PUNCH, or PRINT. If the OP-Code received at STC01 was Read-Repeat, then the variant bits A, I, H, P, X, and C are received. If the OP-Code received at STC01 was either TEST or PAUSE, then the information received at this time has no significance.
STC+1	RC*CHAF*XFROTA	Increment the Status Counter by 1.
STC03		No Action
STC+1	RC*CHAF*XFROTA	Increment the Status Counter by 1.
STC04		Check for TEST or PAUSE OP
PAUSOP←1	RC*CHAF*TEOPF*PUOPF	If the OP-Code received is either TEST or PAUSE, set the PAUSOP Flip-Flop.
STC+1	RC*CHAF*XFROTA	Increment the Status Counter by 1.
STC05		Set Pause delay if Test or Pause OP
STC+1	RC*CHAF*XFROTA	Increment the Status Counter by 1.
PAUSOS←1	PAUSOP	If either TEST or PAUSE OP is true, PAUSOP was set at STC04. PAUSOS 1 indicates a Multi is triggered (TAON) . . . Note that new schematics will not use a Multi but rather a "Register" . . . Reference needed.
PUOPF←0 PRTOPF←0 RDOPF←0	RC*CHAF* XFROTA*PAUSOP	Reset the Punch, Print and Read Flip-Flops as PAUSOP true indicates the operation is either TEST or PAUSE.
STC06		Determine OP-Code
STC+1	RC*CHAF*XFROTA* ((RDOPF*PUOPF/* PRTOPF/) +TEOPF +READYF +PAUSOP +REPRD)	Exit to STC07 to receive the Reference Address (Byte 1) if any of the conditions are met: Read OP and Not Punch or Print . . . Test OP . . . . Device Not Ready . . . . Pause OP . . . . Read-Repeat OP . . . .

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From CTC06

CTC06

STC+8	RC*CHAF*XFROTA* (PUOPF+PRTOPF)* READYF	If the device is ready and the OP Code is either Punch or Print exit to STC14 to receive either Punch or Print data. Note that this exit is also used if the Read OP is also true with either the Punch OP, Print OP, or both.
	STC17	
STC07 + STC08		Receive Reference Address (Bytes 1 & 2)
IR←—EXCH	STC07+STC08* (CA*CH*XFROTA)	Gate the Reference Address (Byte 1 or 2) to the Input Register. Byte 1 is sent during STC07.
STC+1	STC07+STC08* (RC*CHAF*XFROTA)	Increment the Status Counter by 1. After the increment occurs, the STC will equal either 08 or 09.
PH2DY←1	STC07+STC08* (RC*CHAF*XFROTA)	SHF 1 sets the Shift Flip-Flop. SHF is true after the trailing edge of the next DSCP occurs. With SHF true, the four phase delay logic is triggered which causes a shift right by 1 of the 100 byte MOS Register to occur. The data in the Input Register is shifted into the first storage element position of the MOS Register. Each of the 100 byte positions of the Register is also shifted right by 1.
STC09		Receive Reference Address (Byte 3)
IR←—EXCH	CA*CH*XFROTA	Gate the Reference Address (Byte 3) to the Input Register. EXCH lines 07 thru 00 contain byte 3.
STC+1 PH2DY←1	RC*CHAF*XFROTA	Increment the Status Counter by 1 and generate a shift of the MOS Register.
INHFDF ← 1	RC*CHAF*XFROTA* ((SECHOP/*PHE)+ (SECHOP*SHE))	Set the Inhibit Feed Flip-Flop if either the Primary Hopper is selected and empty or the Secondary Hopper is selected and empty. No card is fed from the selected input Hopper. This is used to get the last card of a file out of the Wait Station.
PRIMF ← 1	RC*CHAF*XFROTA* SECHOP/*PHE* RBFF/	If the Primary Input Hopper has been selected and it's empty (PHE), set the PRIMF Flip-Flop. PRIMF is used during STC22 to indicate the empty hopper condition in the Result Descriptor. Note that PREHOP will be true as well as the Exception condition (EXCPT). RBFF/ indicates the device Read Buffer is not full. RBFF/ is also gated because a Read Repeat OP and with data already in the buffer will send data "OK". INHFDF will prevent the feed of a new card from the hopper.
SECF ← 1	RC*CHAF*XFROTA* SECHOP*SHE* RBFF/	If the Secondary Input hopper is selected and it's empty, set the SECF flip-flop. SECF is used during STC22 to indicate the empty hopper condition in the Result Descriptor. The Exception bit is also true as is the reason for RBFF/ stated in the above block.

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From STC09

STC09

LOOPF ← 1	RC*CHAF*XFROTA* PUOPF/*PRTOPF* *RDOPF
FEEDF ← 1	RC*CHAF*XFROTA* READYF*TEOPF/* PAUSOP/*LOOPF/* ((REPRD/)+REPRD* RBFF/))

If this is a Print and Read OP, then set the LOOPF flip-flop. LOOPF is set to enable setting the UNLOADF flip-flop at STC10 line 25 during print and read operations.

Set the Feed flip-flop if the OP-Code is neither TEST, PAUSE, or Read Repeat except when Read Repeat and the Read Buffer is not full (indicates first card only). LOOPF/ indicates this is the first time through. Note that if the operation is Read Repeat, a card cycle is initiated in STC 10 (line 30) after the read data has been loaded and INCSHF is true.

STC10

1	SCCLF ← 1	CCLF/*4US* FEEDF
2 3	SCCLF ← 0 FEEDF ← 0	(4US*CCLF) +READYF/
4	OPSTF ← 1	SCCLF*CCLF
5	RDCKF ← 1	CCLF*RDCK
6	PUNCKF ← 1	CCLF/*4mms* PUNCKD
7 8 9 10	PPIBL/ ← 1 PUOPF ← 1 PPICL/ ← 1 PRTOPF ← 1 SS4L/ ← STR4 SS2L/ ← STR2	UNLOADF/

Start Card Cycle Level will initiate feeding a card from the Input Hopper, through the Read Station to the WAIT Station. The card at the WAIT Station (if any) will also move through the Punch & Print Stations to the selected stacker. CCLF/ insures a card cycle is not in progress and the FEED F/F is set during STC09 if the OP Code is Not Test, Pause or Read Repeat. Read Repeat is conditional on the Status of the Read Buffer – Refer to STC09.

When the device sends CCL/ . . . 1 indicating a card cycle is in progress, CCLF is set in the Control. The Ready F/F is reset causing READYF/ to be true if the device is not ready.

When SCCLF and CCLF are true it indicates the Device has received the Start Card Cycle level and has responded by initiating a card cycle. The Operation Start F/F is set to indicate at STC13 that a card cycle was initiated; therefore, exit can be made to STC15 to send the Read Data if a read is designated.

If a read error is detected by the Device during the reading of a card, the Read Check F/F is set. RDCKF . . . true will cause the error condition to be flagged in the Result Descriptor.

If a Punch Check is detected within the Device, the Punch Check level PUNCK/.1) is sent to the Control. Although the device will gate the card in error to the error stacker, the error is not flagged until the operation is complete (CCLF/true). Therefore, a Result Descriptor containing the Punch check bit is not sent until the completion of the next card cycle. 4mms = 4us clock.

The Unload flip/flop when set is used to unload Punch or print data to the Device via the eight PPIXL lines. When the unload F/F is reset (UNLOADF/ true) the PPIXL lines are used to send the Punch and a Print OD to the Device, as well as the stacker select, secondary hopper, second path, different panel/print data and/or Inhibit feed. Five of the PPIXL lines are therefore time shared.

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From STC10

STC10

11 12 13 14 15	SS1L/ ← STR1 PAUSOP ← 1 SECHOP ← 1 PPI8L/ ← 1 SECPAH ← 1 SPRINL/ ← 1 DIFF ← / PPIDL/ ← INHIBIT	UN LOADF/	
16	INCSHF ← 1	LOADF*BCNT96* PH1DY	Setting the Incomplete Shift F/F (INCSHF) will cause the 8 x 100 mos register to be right justified. One shift will occur with each 4us clock pulse.
17		+(SCCLF*4US*CCLF *(PUOPF+PRTOPF)	Line 17 is true when 96 characters of read data from the device is in the MOS Register.
18		+LOOPF*BCNT96*4US	Line 18 is true when a Punch or Print operation is initiate. Setting INCSHF enables unloading the Punch or Print Data to the Device. Refer to line 25.
19		+ TEOPF/*PAUSOP/ *READYF/*4US	Line 19 has significance if this is the second time through STC10. As the LOOPF F/F will have been set at STC13 with PUNCH, Print, *DIFF TRUE.
20		+PAUSOP*PAUSOS/* 4US	Line 20 indicates Not a Test OP or Pause OP and the Device is Not Ready.
21		+TEOPF*((RDOPF* READYF)+ (WNOTRF*READYF/)+ (WNOTRF/* RDOPF/)*4US	Line 21 indicates it is a test OP and one of the following is true: 1. RDOPF*READY*RDOPF indicates WAIT until Ready & Ready indicates the Device is ready. 2. WNOTRF*READYF/*WNDTRF indicates wait until Not Ready & READYF/ indicates the Device is Not Ready. 3. (WNOTRF/*RDOPF/) Test immediately for all conditions.
22	PH2DY ← 1	INCSHF*4US	When the INCSHF F/F is set, each 4us clock pulse causes SHF . . . . 0 to be true. SHF ←‾‾ 0 true generates PH2DY CTL-P#1, PH1DY & CTL-PH2 in sequential order. Each is true for one clock period except CTL-PH2 which remains true until the next SHF . . . . 0 occurs. The result of the 4 outputs of the shift phase generator is one complete shift right by 1 bit position of each 8 bit character in the 100 bit MOS Register.
23	BCNT+1 STCS10 ← 1	PH2DY	PH2DY is the first output of the shift phase generated triggered by SHF ←‾‾. 0. The Byte Counter is incremented by 1.
24	OR ← BUF	INCSHF* BCNT97*4US	When BCNT = 97 it indicates the data is Right Justified in the 100 Bit MOS Shift Register, the 4us clock will also cause another shift to occur which will upcount the Byte counter to 98. The output bit position of the MOS-Register (BUF 00-07) are set into the Output Register (OR 07-00)

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From STC10 From STC10

25	UNLOADF ← 1	INCSHF*BCNT98* PH1DY*READYF* ((LOOPF)+(LOOPF/* PUOPF*PUDONEF/)+ (RDOPF/*REPRD/))	The UNLOADF F/F is set to allow gating the contents of the MOS Register to the PUNCH/Print Buffers in the Device. Refer to times 31 through 39. BCNT98 is true for 2 clock periods as BCNT is set to zero at line 28. Only Punch and/or Print Operations will cause UNLOADF to be set.
26 27	STC+1 SRF ← 1	INCSHF*BCNT98* PH1DY* ((PUOPF/*PRTOPF/)+ (LOOPF/*PUOPF/* RDOPF)+(TEOPF)+ (PAUSOP)+(READYF/)+ (PUOPF*PUDONEF))	INCSHF*BCNT98*PH1DY true indicates an 8-Bit Character is in the output Register and the output bit position of the MOS Register (BUF 07-00) contains the next character. The logic in ( ) indicats the first Byte of the Ref address is in the output Register (OR) and the 2nd and 3rd Bytes of the Ref address is in the last and next to last output position of the MOS Register. PUOPF/* PRTOPF/ indicate Read or Read Repeat. LOOPF/*PUOPF/* RROPF indicates Print & Read. TEOPE indicates Test OP. PAUSOP indicates Pause OP. READYF/ indicates "any" OP and Device Not Ready. PUOPF*PUDONEF indicates a Punch & Read or a Punch/Print & Read and Not Diff. → STC11
28 29	BCNT ← 00 INCSHF ← 0	INCSHF*BCNT98* PH1DY	The Punch or Print Data or the Ref Address in the MOS Register is Right Justified with one character in the output Register. The Byte counter is reset to zero to insure the Byte counter will increment to 96 during the UNLOAD operation. As Data is right Justified, INCSHF is reset.
31	PPINLF ← 1	UNLOADF*PPINL*1US	When Punch/Print Information Needed level is received from the Device, set PPINLF if a PUNCH or Print operation is designated by UNLOADF true.
32	XCPU ← 1	PPINLF*UNLOADF*1US	Set the transfer clock Pulse (XCPU) FF when PPINLF is set. XFRP/ is sent to the Device.
33 34	BUS ← OR PPIXL ← BUS	UNLOADF	Gate the contents of the output Register (0R00-07) to the Punch Print Information levels (PPIXL)
35	PPINL ← 0	XCPU	The Device will reset PPINL in the Device when XCPU is set. PPINL--0 will cause PPINL/ to be true.
36	PPINLF ← 0	PPINL/*1US	Reset PPINLF when PPINL/ is true.
37	SHF← 0 PH2DY	PPINL/*XCPU*1US* UNLOADF	Set the output Buffer of the MOS Register (BUF00-0) into the Output Register and generate a shift of the 8 x 100 bit MOS Register.
38	OR← BUF	PRINL/*CTL-PH1 *UNLOADF	
39	XCPU←0	1US*PPINL/	Reset the Transfer clock pulse FF and wait for the next PPINL from the Device at line 31.
40	CIRCF ← 1	BCNT96*PH1DY* UNLOADF*INHIBT/* *((PUOPF*PRTOPF/ *RDOPF)+(PUOPF/*PRTOPF *RDOPF)+(PRTOPF*RDOPF *DIFF/))	The circulate F/F (CIRCF) is set to gate the 3 Bytes of the Reference Address from the output of the MOS Register to the Input of the MOS Register. Refer to Lines 52 through 59. If the feed of a card from the Input hopper is not designated (INHIBT/false) the Reference Address is not circulated as a Read OP would be redundant.

CONTINUED ON NEXT PAGE

STC10	From STC10	
41	STC+8	BCNT96*PH1DY* UNLOADF*
42	SRF←1	INHIBT* ((PUOP*PRTOPF/ +(PUOPF/*PRTOPF* RDOPF/)+(PRTOPF* DIFF/))
43	CRBFF←1	BCNT96*PH1DY* UNLOADF*INHIBT/*
44		+(PUOPF*PRTOPF/* RDOPF/)+
45		+(PUOPF*PRTOPF/* RDOPF/)+
46		+(PUOPF/*PRTOPF* RDOPF/)+
47	STC+1	BCNT96*PH1DY* UNLOADF*
48	SRF←1	PUOPF*PRTOPF* DIFF
49	BCNT←00	BCNT96*PH1DY* UNLOADF
50	UNLOADF←0	
51	PPINL←1	XCPU/
51A	BUS←OR	CIRCF
52	OR←BUF	CIRCF*CTL-PH1
		CIRCF*4US
53	IR←OR	
54	PH2DY	
55	BCNT+1	PH2DY
56	LOOPF←0	BCNT03*PH1DY* CIRCF
57	CIRCF←0	
58	BCNT←00	
59	PUDONEF←1	

INHIBT true indicates a card was not fed from the Input Hopper; therefore, there is NO read data available. When BCNT96 is true the Punch and/or Print Data has been transferred to the Device. Exit to STC18 to send the reference address. The service Request F/F is set to signal the Processor to initiate a transfer in command to receive the Reference Address. PUOPF*PRTOPF/ indicates Punch OP or Punch & Read Op. PUOPF/*PRTOPF*RDOPF/ indicates Print OP. PRTOPF*DIFF/ indicates Print * Punch OP & "same" or Print, Punch & Read OP and "same" or Print & Read.

STC18

Clear Read Buffer Full (CRBFF) F/F will cause the read buffer in the Device to be cleared. With INHIBT/true, a card is fed from the Input Hopper with SCCL and a read of that card by the Device will occur. The conditional logic indicates (PUNCH OP)+(Print OP)+ (PUNCH*Print*Diff, "second time through STC10")) + (PRINT* PUNCH*"SAME") Note that None indicate a Read OP.

BCNT96*PH1DY indicates the Punch Data has been transferred to the Device. As Different Punch & Print Data is specified, exit to STC11 to enable sending the Punch data's reference address where the Service Request is recognized by the Processor.

STC11

Reset the Byte Counter and the UNLOADF F/F as the Print or Punch Data has been transferred to the Buffer in the Device.

If the data transfer operation is not complete, the Device will send PPINL to the control when the Transfer Clock Pulse F/F (XCPU) is reset. XCPU/ will send XFRP/ (false) to the Device.

When the Circulate F/F is set, each 4us clock pulse will gate the Output Register (OR00-07) to the Input Register (IR00-07) and a shift of the 8 x 100 bit MOS Register will occur.

PH2DY occurs for one clock period following the clock period SHF . . . . 0 is true. Refer to STC "Any". As a shift of the MOS Reg. is indicated, upcount the Byte Counter by 1 to count the shifts.

The logic indicates the Reference Address has been circulated from the Output Reg to the Input Register of the MOS Register & the 3 bytes of the Reference Address are in the MOS Register. If LOOPF is set due to a Punch/Print/Diff operation then reset it. CIRCF is reset as the circulate operation is complete. BCNT is reset to zero in preparation of receiving the Read Data. PUNCH Done (PUDONEF) is set to indicate (line 26 & 27) that the Punch operation (if applicable) is complete.

CONTINUED ON NEXT PAGE

STC10		From STC10	
60	LOADF ←1	BCNT03*PH1DY* CIRCF*INHIBT/	The Load F/F is set to enable loading the read data from the read Buffer in the device to the Input Register and to the MOS Shift Register. Refer to lines 65-87. Three conditions will set LOADF. 1. A circulate of the Reference address is complete and a card from the input hopper has been fed. 2. The Read Buffer is full and this is a Read or Read Repeat operation. Note that although BCNT00 is true, the Reference Address is in the left most character position of the MOS Register. STCS10 is set when PH1DY*STC10 are true. It is reset with STC10/. The PH1DY will occur as the result of a shift at STC09. 3. The Load F/F is set with CRBFF*BCNT00*1us*RIALF only to allow the Device to complete a PUNCH and a Print Operation. It is redundant within the control as Clear Read Buffer will be sent.
61		+RBFF*INHBT/* STCS10)*1US* BCNT00*PUOPF/* PRTOPF/*((RDOPF* TEOPF/)+REPRD))	
62		+CRBFF*BCNT00*1US* RIALF	
63	INCSHF ←1	BCNT03*PH1D/* CIRCF*INHIBT	The first conditional logic is set INCSHF indicates the Reference Address has been recirculated however with INHIBT true a card will not be fed; therefore, there is no Read Data. INCSHF is set to Right Justify Reference Address in MOS. The second conditional logic indicates a Read or Read Repeat operation is specified. However, a card is not fed and read; therefore, set INCSHF to right justify the Reference Address.
64		+BCNT00*1US*PUOPF/* PRTOPF/*((RDOPF* TEOP/)+REPRD) * INHIBT	
64A	OPSTF←1	LOADF	
65	RBFF ←1	RBFL*1US	When the Read Buffer Full Level (RBFL) is received from the Device set RBFF in the control.
66	RBFF ←0	RBFL/*1US	Reset RBFF when the Device no longer sends RBFL.
67	RIALF ←1	RIAL*1US	When RIAL is received from the device indicating Read Information available, set the RIALF (F/F) in the control.
68	PH2DY←1	LOADF*CRBFF/* RIALF*XFRP/*1US	XFRP/ true indicates XFRCP is false. Generate a shift of the MOS Register.
69	XFRCP←1	LOADF*RIALF*1US* CRBF/*XFRCP/	Set the Transfer Clock Pulse F/F (XFRCP) when RIALF is set. XFRCP/ is sent to the Device.
70	IR←CODE 6	LOADF*RIALF* XFRCP/*1US*CRBFF/* CODE6	Code 6 indicates the Translator is to be bypassed. The Read Data on the RDIX6 lines is gated directly to the Input Register (IR).
71	IR←RDIXL		CODE6/ indicates the Translation to be used. The Output of the Translator (ECnL) is gated to the Input Register (IR). Note that the Read Data on the RDIXL lines is gated to the Translator.
72	CLRF ←1	LOADF*RIALF* XFRCP/*1US*CRBFF	When CRBFF is set (line 43) the Clear Read F/F (CLRF) is set.

CONTINUED ON NEXT PAGE

Functional Detail

STC10	From STC10	
73	CLRRDBF	CLRF
74	BCNT+1	PH2DY
75 76	INVALF←1 INHFDF←1	LOADF*BCNT01* PH1DY*CODEQM
77	RIAL←0	XFRCP+CLRDBF
78	RIALF←0	RIAL/*1US
79 80 81	LOADF←0 STC+8 SRF←1	CLRF*RIALF/*1US
82	XFRCP←0	RIAF*1US
83 84	CLRF←0 CRBFF←0	RIALF/*LOADF *1us
86	INCSHF←1	LOADF*BCNT96* PH1DY
85	LOADF←0	STC10/+(BCRT96 *PH1DY)
87	RIAL←1	XFRCP/

When CLRF is set, send Clear Read Buffer (CRBF/ false) to the device.

Upcount the Byte counter by 1 when a shift of the MOS Register occurs. Refer to STC "Any" for PH2DY timing.

If the "?" is detected in column 1 of the card, the INVALF F/F and the INHFDF F/F are set, a validity check is flagged in the Result Descriptor and the card is left in the Wait Station and no additional card is fed.

The Device will upon receiving either the Transfer Clock Pulse or the Transfer Clock Pulse or the Clear Read Buffer level will terminate sending RIAL.

When RIAL goes false (device dependent) the Control will reset RIALF with the next 1us clock pulse.

Set the Service Request F/F (SRF) reset LOADF AND exit to STC18 if CLRF is set. Refer to lines 43 & 72.

STC18 →
Reset the F/F prior to receiving the first RIAL which will set RIALF.

The conditional logic indicates the load is complete. Reset the Load F/F and set INCSHF in preparation of Right Justifying the Data in the MOS Register.

The Device will send RIAL if the load is not complete.

STC11 or STC12	
EX←BUS BUS←OR	CHAF*XFRIN
PH2DY←1	RC*CHAF*XFRIN
OR←BUF	PH2DY*XFERIN
STC+1	RC*CHAF*XFRIN
STC11	
SFR←0	RC*CHAF*XFRIN
STC13	
EX←BUS BUS←OR	CHAF*XFRIN

Send Reference Address (Bytes 1 & 2)

Gate Output Register to Exchange 00-07

Shift MOS Register right by 1 Gate Output of MOS to Output Register Increment STC by 1

Reset the Service Request Flip-Flop

Send Reference Address (Byte 3)

Gate Output Register to Exchange 00-07

CONTINUED ON NEXT PAGE

From STC13

STC13

PUOPF←0		Shift MOS right by 1 Gate Output of MOS to Output Register Reset the Punch OP Flip-Flop.
OR← BUF	PH2DY*XFRIN	
PRTOPF←0	RC*CHAF*XFRIN* PUOPF/	If a Punch OP was not designated, then reset the Print and Read OP Flip-Flops.
STC+1 LOOPF←1	RC*CHAF*XFRIN* READYF*PUOPF* PRTOPF*DIFF	→ STC 14 If this is a Punch and Print OP and the Punch and Print data is different, exit to STC14 to receive Punch or Print data. LOOPF is set to indicate at STC09 that a second pass through STC10 will occur, therefore, the feed Flip-Flop is not to be set.
STC+2 PH2DY←1	RC*CHAF*XFRIN* OPSTF* ((PUOPF/*RDOPF)+ (PRTOPF/*RDOPF)+ (RDOPF*DIFF/)+REPRD	→ STC 15
STC+8	RC*CHAF*XFRIN* (TEOPF+ OPSTF/)+ PAUSOP)	→ STC 21

STC 13 + 06

STC14 — Receive Punch or Print Data

IR ← EXCH	CA*CH*XFROTA	Gate the Exchange lines 00 thru 07 to the Input Register.
PH2DY←1	RC*CHAF*XFROTA	Shift the MOS Register right by 1.
BCNT+1	PH2DY	Increment the Byte Counter by 1
STC ←17	RC*CHAF*XFROTA* BCNT94	→ STC 17 When the Byte Counter is equal to 94 and another Transfer Out command is received, a shift also occurs which will increment BCNT to 95. Exit to STC17 to receive the last character.

STC 13

STC 15 — Send Read Data to the Processor

PH20DY	RC*CHAF*XFRIN	Gate the output of the MOS Register to the Output Register. Shift the MOS Register right by 1.
OR←BUF	PH2DY*XFRIN	
EX ← BUS BUS ←OR	CHAF*XFRIN	Gate the OR Registers contents to the Exchange lines 00 thru 07.
BCNT+1	PH2DY	Increment the Byte Counter by 1
STC←17	RC*CHAF*XFRIN* BCNT96	When the Byte counter is equal to 94 and another Transfer In command is received, a shift of the MOS Register also occurs which will increment the Byte counter to 95. Exit to STC17 to send the last Character to the Processor.

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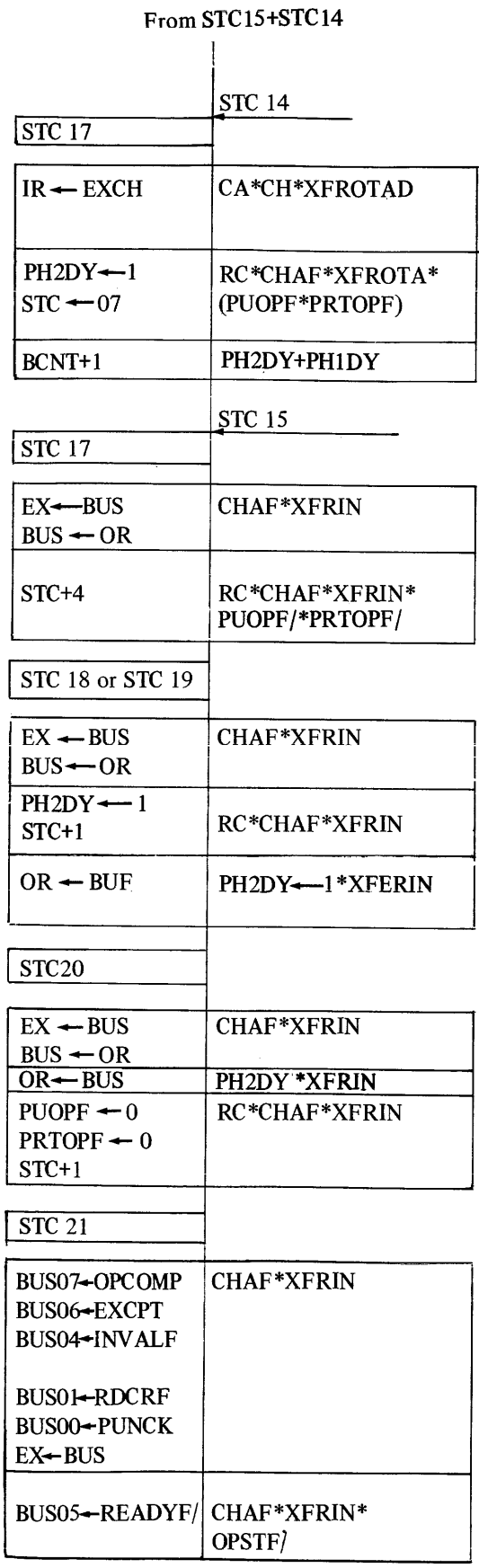
Functional Detail



Receive last Punch or Print Data

Gate the Exchange lines 00 thru 07 to the Input Register.

Shift the MOS Register right by 1 only if either PUOPF or PRTOPF and exit to STC07 to receive the Reference Address.

The Byte Counter is incremented to 96.

Send last Read Data to the Processor.

Gate the contents of the Output Register (last character of read data) to the Exchange lines 00 thru 07.

If this is not a Punch or Print OP then exit to STC21 and send the Result Descriptor to the Processor.

Send Reference Address (Byte 1 & 2)

Gate the Output Register to the Exchange lines 00 thru 07.

Shift the MOS Register right by 1

Gate the output of the MOS Register to the Output Register and increment the Status Counter by 1

Send Reference Address (Byte 3)

Gate the Output Register to the Exchange lines 00 thru 07

Reset the PUOPF & PRTOPF, operation is complete . . . . exit to STC 21 and send Result Descriptor.

Send Result Descriptor (Byte 1)

OP-Complete bit
If and exception is true
INVALF indicates a ? was found in the first column of read data (?character)
Read Check
Punch Check

Not Ready . . . operation not performed

CONTINUED ON NEXT PAGE

From CTC10

INHFDF←1	REPRN*(RDCKF+INVALF)	
STC+1	RC*CHAF*XFRIN	Exit to STC22 and send Result Descriptor Byte 2
STC 22		Send Result Descriptor (Byte 2)
BUS07←PREHOP BUS06←SECEHOP EX←BUS	CHAF*XFRIN	Primary Hopper Empty Secondary Hopper Empty
STC+1	RC*CHAF*XFRIN	Exit to STC23 and send last byte of Result Descriptor.
STC 23		Send Result Descriptor (Byte 3)
BUS ← ID	CHAF*XFRIN* (TEST+PAUSOP)	If this was either a TEST or Pause OP then send the Control Identification to BUS 06 thru 01.
BUS← 0C EX ←BUS	CHAF*XFRIN	Send OP-Complete on BUS 07 Gate BUS 07 thru 00 to Exchange 07 thru 00
STC ← 01 BCNT ← 00 INVALF ← 0 PUNCKF ← 0 RDCKF ← 0 PRIMF ← 0 QPREG ← 0 PUDONEF ← 0 CRBFF ← 0 LOOPF ← 0 PAUSOP ← 0 INHFDF ← 0 SECF ← 0 OPSTF ← 0	RC*CHAF*XFRIN	Exit to STC01 and await another command Execute a "general" clear of Registers, Counters, & Flip-Flops
SCCLF←1	RERRD*CCLF/	Send another SCCL if in Read Repeat

End of Flow

Adjustments

SECTION IV

There are no adjustments for the 96 column Multi Function Card Unit Control.
Refer to I/O Base Section IV for clock adjustments.
Refer to 96 Column Multi Function Card Unit Control Section VI for determining the control channel number.
Refer to 96 column Multi Function Card Unit Control Section VI for instructions for wiring the ID jumper chip.

INTRODUCTION

The purpose of this section is to provide directions and aids in maintaining the 96 Column Multi Function Card Unit Control.

PREVENTIVE MAINTENANCE

There is no preventive maintenance for the 96 column MFCU Control. Refer to B9419 Technical Manual for the Interpreting Data Recorder PM.

SPECIAL MAINTENANCE TOOLS REQUIRED

96 Column Test Routines
B 1700 Field Card Tester
Tektronix 453A Oscilloscope or equivalent
Tripplet 630 VOM or equivalent

MAINTENANCE CONCEPT

B 1700 controls are soft controls. No offline capability is built into the control. The B 100 Maintenance concept is centered around the use of test routines used in conjunction with the Field Card Tester. Hardware testpoints are provided for conventional troubleshooting.

TEST ROUTINES

CONFIDENCE ROUTINE

96 column MFCU Confidence Routine tests the following.

1. Punches and prints 150 cards of alpha-numeric data. First card has A in column one and continues through the alphabet, then numbers 0 through 9 followed by the special characters. This sequence is repeated until 96 columns are filled. The number 6 is the last character punched on card 1. Card 2 will start with the number 6 in column one and ends with the number 5. The Field Engineer must verify the print operation by comparing the first card with Figure V-1.

2. The previous punched deck is removed from the stacker and placed in hopper one. The program reads the deck and compares the data read with the data sent to the punch in step one. If a difference is detected the program halts with the card in question at the wait station.

   The processor halts with the following information available:

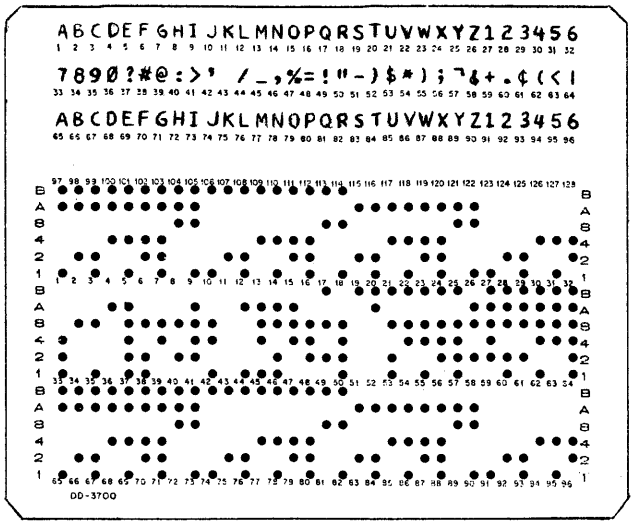
   1. The T Reg. contains the expected character.
   2. The Y Reg. contains the bad character.
   3. The L Reg. contains the failing column.
   4. The FA Reg. contains the tank address.
      (S-Mem. Address where data is stored)

NOTE: The program will halt when the card having a question mark in column one is read. This checks the validity error circuit in the control.

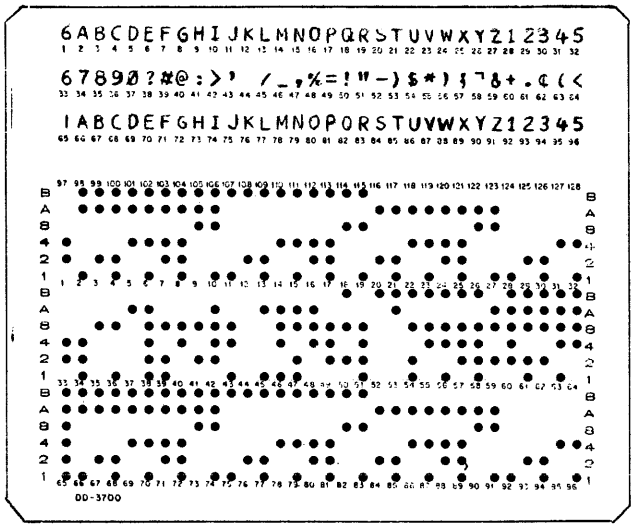
3. The original deck is placed in the hopper #1. Two hundred (200) blank cards are placed in the hopper #2. The program reads the card from the hopper #1 and punches and prints a blank card from hopper #2 with identical information. As in step 1 the print must be verified by the operator. This routine fully exercises the control and peripheral.

4. Remove newly punched deck from stacker 2 and place in hopper 1. The cards are checked in the same manner as step 2.

CARD 1



CARD 2



CARD 3

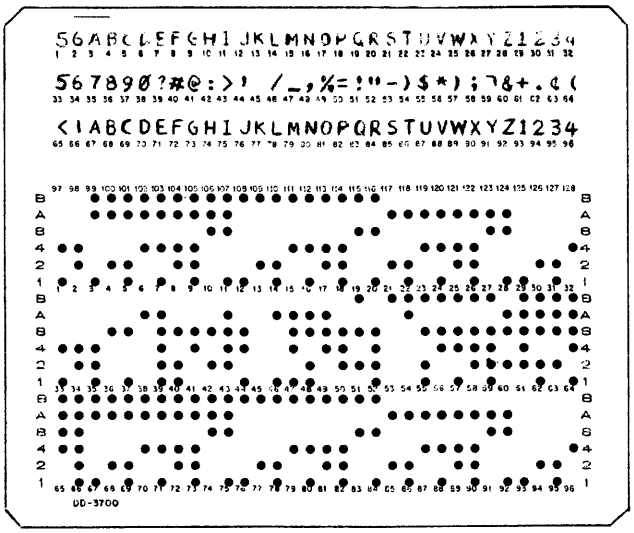


Fig. V-1 CONFIDENCE ROUTINE PUNCHED DECK

HOW TO LOAD TAPE

1. Place Processor in the MTR mode and Ready the B9419.

2. Insert the 96 column MFCU confidence routine into the Cassette Drive.

3. Clear FA-Reg and Depress START.

4. After the cassette halts, place the processor in the RUN mode and again depress START.

RUN INSTRUCTIONS

1. The 96 column MFCU Confidence Routing Listing gives run instructions.

2. Basically this will involve removing the cards from the stacker and placing them in the proper hopper. After loading cards the Start button on the console must be pushed.

RESULTS

Refer to Test Procedures to analyze the failure.

I/O DEBUG ROUTINE

GENERAL

Figure V-2 is a breakdown of the Processor to I/O flow. The I/O Debug Routine is a basic routine that follows the path shown in the figure. This routine may be used for any I/O Control. The OP Code and control channel number have to be manually loaded. The instructions on the program listing give the FA value where these commands are placed.

STEPPING

By stepping this program 1 micro at a time the Field Engineer can observe Hardware testpoints and determine the internal 96 column MFCU control operation.

Each time this program sends out a basic command to the I/O it will read in the status of the 24 exchange lines to the L Reg. By displaying L at the proper time the Field Engineer can observe what status count the control is at and what data is returned to the processor. By looking at the T Reg. at the proper time the Field Engineer can observe the commands and data sent to the control.

USING HALTS

Figure V-2 shows the basic subroutines within the boxes. For example, send OP Code is a sub routine. The Debug program has no-op micros placed between subroutines and within certain routines. These allow the Field Engineer to manipulate the program to his liking. For example, a halt could be put after the 1st byte of REF ADD has been transferred to the control. The Field Engineer could then check at the storage buffer in the control for this byte of data. Another example would be placing a halt after the first result Descriptor Byte is transferred in. The L Reg could then be checked for the data.

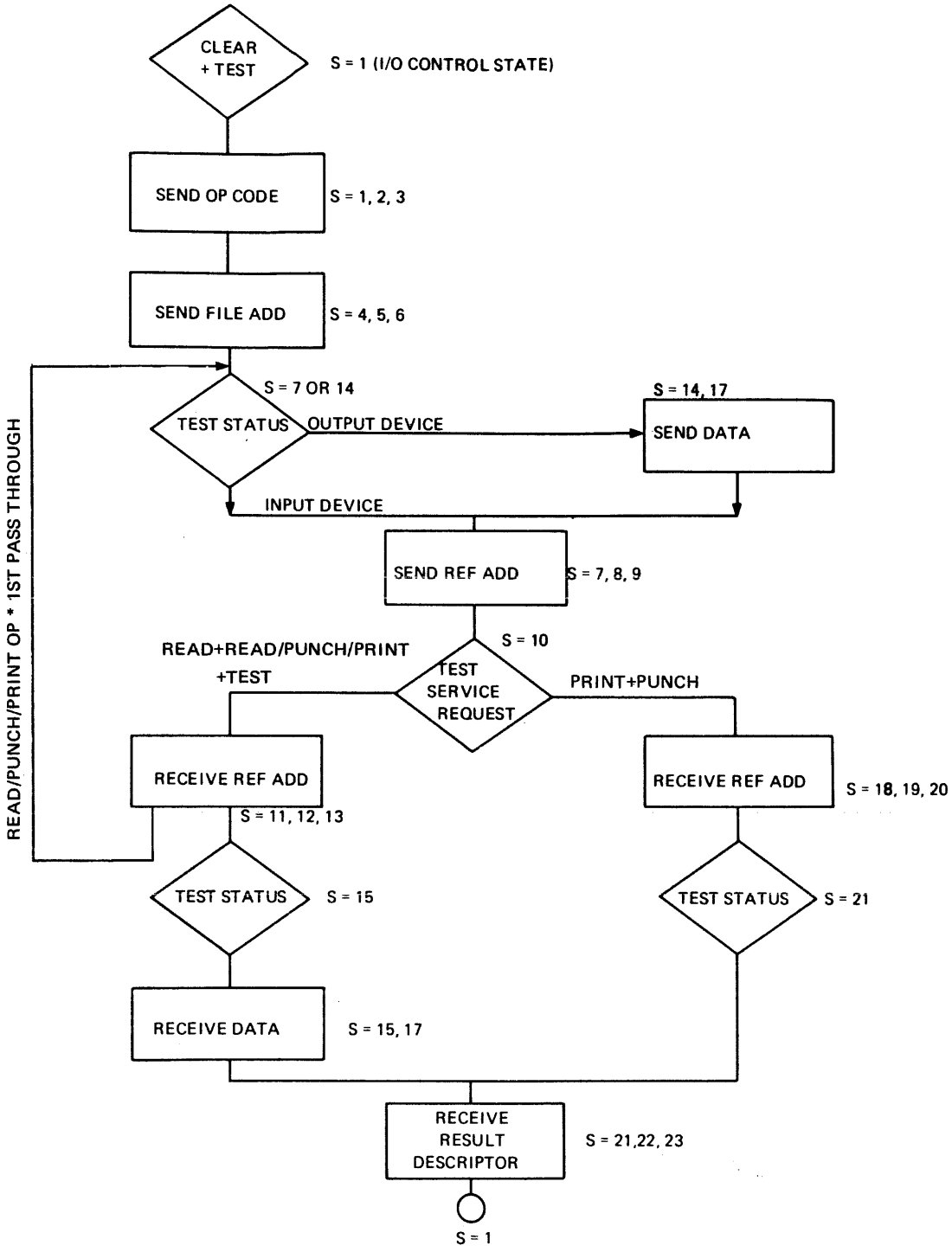


Fig. V-2 PROCESSOR TO I/O FLOW

TEST PROCEDURES

96 Column MFCU Control Troubleshooting should follow these basic steps.

VISUAL CHECKS (REFER TO 96 COLUMN MFCU CONTROL SECTION VI)

1. Assure that the control has been loaded into a valid two card control slot.
2. Assure that the B9419 cabling to the control is proper.
3. Assure that a channel jumper chip has been installed and that no two controls have the same channel number.

RUN CONFIDENCE ROUTINE

1. Before running 96 Column MFCU confidence routine be assured that the Processor and Memory are functioning properly. If necessary run the processor and memory confidence routines.

2. Run the 96 Column MFCU confidence routine (refer to paragraph on Confidence Routine).

TYPE OF FAILURES FROM THE CONFIDENCE ROUTINE

1. Routine will not run
2. Not Ready Section fails
3. Printer fails (visual check of card)
4. Punch fails
5. Read fails
6. Read/Interpret/Punch fails
7. Confidence test passes

DECISION

1. If confidence test passes, attempt to recreate original problem.
2. For a failure. Proceed to the Field Card Tester.
3. Test cards in the Field Card Tester (refer to B 1700 Field Card Tester Manual).
4. If the problem is found and repaired, rerun Confidence Routine.
5. If cards check OK in tester or the problem cannot be resolved, go to next paragraph.

USE OF I/O DEBUGGING ROUTINE

This step involves the running of an I/O Debugging Routine. For operation of the I/O Debugging Routine refer to the paragraphs describing it.

Attempt to analyze the failure of the Confidence Routine and relate it to particular circuitry of the 96 Column MFCU Control.

For example, if the reader failed to read a card properly the problem would likely be on card 1, reader decoder or interface.

PROCESSOR TO I/O TRANSFER PROBLEMS

With problems involving processor to I/O transfers it is best to step the processor and observe hardware testpoints along with processor registers.

HARDWARE TEST POINTS

96 COLUMN MFCU CONTROL CARD 1 FRONT PLANE CONNECTORS

$X
Testpoints

A	RDOPF . . 1	I	ONCTV . . 1	R	IREX3 . . 1
B	REPRD . . 1	J	CA 1	S	IREX4 . . 1
C	INHFD . . 1	K	TSR 1	T	IREX5 . . 1
D	CODE6 . . 1	L	CLTS . . . 1	U	IREX6 . . 1
E	CKOP . . . 1	M	TSTA . . . 1	V	IREX7 . . 1
F	XFERIN . 1	N	IREX0 . . 1	W	RC-CHAF1
G	YFROTB . 1	P	IREX1 . . 1	X	
H	XFROTA . 1	Q	IREX2 . . 1	Y	
				Z	

#X
Testpoints

A	RDIDB . . 1	I		R
B	RDICB . . 1	J		S
C	RDIBB . . 1	K		T
D	RDIAB . . 1	L	REY 1	U
E	RDI8B . . 1	M	RBL 1	V
F	RDI4B . . 1	N	RIL 1	W
G	RDI2B . . 1	P	RDCK . . . 1	X
H	RDI1B . . 1	Q		Y
				Z

$Y
Levels to Card 2 Frontplane Connector $Y

A	OR7 1	I	STC16R . 1	R	BCNT96 . 1
B	OR6 1	J	STC8R . . 1	S	BCNT97 . 1
C	OR5 1	K	STC4R . . 1	T	BCNT98 . 1
D	OR4 1	L	STC2R . . 1	U	XCPU . . . 1
E	OR3 1	M	STC1R . . 1	V	EX ID . 1
F	OR2 1	N	BCNT00 . 1	W	RDCKF . 1
G	OR1 1	P	BCNT01 . 1	X	INVALF . 1
H	OR0 1	Q	BCNT03 . 1	Y	SRF 1
				Z	

Y#
Levels to Reader Portion of MFCM

A	SCCL/ . . 1	I	RDIDL/ . 1	R	RIAL/ . . 1
B	RDI1L/ . 1	J		S	XFRCP/ . 1
C	RDI2L/ . 1	K		T	RBFL/ . . 1
D	RDI4L/ . 1	L		U	RDCHK/ . 1
E	RDI8L/ . 1	M		V	IHINFD/ 1
F	RDIAL/ . 1	N	READY/ . 1	W	
G	RDIBL/ . 1	P	CCL/ . . . 1	X	CRBF/ . . 1
H	RDICL/ . 1	Q	CLEAR/ . 1	Y	
				Z	

96 COLUMN MFCU CONTROL CARD 2 FRONTPLANE CONNECTORS

$X
Testpoints

A	PUOPF . . 1	I	STR1 . . . 1	R	BC16 . . . 1
B	PRTOPF . 1	J	STC16RT 1	S	BC08 . . . 1
C	TEOPF . . 1	K	STC8RT . 1	T	BC04 . . . 1
D	DIFF . . . 1	L	STC4RT . 1	U	BC02 . . . 1
E	SECHOP . 1	M	STC2RT . 1	V	BC01 . . . 1
F	SECPAH . 1	N	STC1RT . 1	W	
G	STR4 . . . 1	P	BC64 . . . 1	X	
H	STR2 . . . 1	Q	BC32 . . . 1	Y	
				Z	

Maintenance Procedures

#X
Testpoints

A	CCL....1	I	R
B	READY .1	J	S
C	PHE....1	K	T
D	SHE....1	L	U
E		M	V
F		N	W
G		P	X
		Q	Y
			Z

$Y
Levels to Card 1 $Y

A	OR7....1	I	STC16R .1	R	BCNT96 .1
B	OR6....1	J	STC8R ..1	S	BCNT97 .1
C	OR5....1	K	STC4R ..1	T	BCNT98 .1
D	OR4....1	L	STC2R ..1	U	XCPU ...1
E	OR3....1	M	STC1R ..1	V	EX ID .1
F	OR2....1	N	BCNT00..1	W	RDCKF ..1
G	OR1....1	P	BCNT01..1	X	INVALF .1
H	OR0....1	Q	BCNT03..1	Y	SRF 1
				Z	

#Y
Levels to Punch-Printer Portion of MFCM

A	SCCL2/.1	I	PPIDL/ .1	R	PPINL/ .1
B	PPI1L/ .1	J	SPRINL/.1	S	XFRP/ ..1
C	PPI2L/ .1	K	SS1L/...1	T	
D	PPI4L/ .1	L	SS2L/...1	U	PUNCK/ .1
E	PPI8L/ .1	M	SS4L/...1	V	PREHOP/.1
F	PPIAL/ .1	N	READY/.1	W	SCEHOP/ 1
G	PPIBL/ .1	P	CCL/....1	X	
H	PPICL/ .1	Q		Y	SCCL2/ .1
				Z	

BACKPLANE CONNECTOR
96 COL. MFCU CONTROL CARDS

	0		1
	+4.75	A	+4.75V
	EXCH00 .0	B	EXCH01 .0
	EXCH02 .0	C	EXCH03 .0
	EXCH04 .0	D	grnd
	EXCH05 .0	E	EXCH06 .0
	EXCH07 .0	F	
		G	
		H	
		I	
		J	grnd
X Connector	EXCH16 .0	K	EXCH17 .0
	EXCH18 .0	L	EXCH19 .0
	EXCH20 .0	M	EXCH21 .0
	EXCH22 .0	N	
	CIRCF . .0	P	CCL 0
	4US 0	Q	grnd
	1US 0	R	STCS10 .0
		S	UPSTF/ .0
	1024us .0	T	PHOPE . .0
	SHOPE . .0	U	CRBFF . .0
	LOOPF . .0	V	
	SCPM . . .0	W	grnd
	PRTOPF .0	X	PUNCKF .0
		Y	WNOTRF .0
		Z	PUOPF . .0
		A	
	TEOPF . .0	B	MOS 0
	INHFD . .0	C	CLRB . . .0
	SHF . . .0	D	grnd
	PPINLF .0	E	RC 0
	READY . .0	F	CA 0
	UNLODF .0	G	SR 0
	CHAF . .0	H	
	INCSHF .0	I	PWRON . .0
Y Connector	PAUSOP .0	J	grnd
	RC-CHAP 0	K	RDOPF . .0
	READYF .0	L	
	REPRD . .0	M	TSR/ . . .0
	XFERIN .0	N	TESTER .0
	XFROTA .0	P	XFROTB/ 0
	CLRF . .0	Q	grnd
	LOAD . . .0	R	PH2DY . .0
	RBFF/ . .0	S	RIALF . .0
	XFRCP . .0	T	CA-CH . .0
	CCLF . . .0	U	INHIBT .0
	SCCLF . .0	V	XFROTAD 0
	CLTS . . .0	W	grnd
	INHFDS .0	X	PH1DY . .0
	RDCK . . .0	Y	SCCL/ . .0
	-2V	Z	-2V

Installation Procedures

INTRODUCTION

This section provides information to install and check out a 96 Column Multifunction Card Unit control.

LOGIC PREPARATION

The processor communicates with an I/O control by addressing the controls unique channel number. During a service request by a control the channel is used to determine priority in the event two or more controls need service. Priority is determined by high order number first. Channel number for a particular control will vary depending on system configuration.

The 96 Column Multifunction Card Unit control is capable of controlling a number of 96 column devices. These are listed in Table I-1 of Section I. The control reports the identity of the device insofar as punch/print/read capability.

CHANNEL NUMBER ADJUSTMENT

Jumper chip A9 of Card 1 should be wired to reflect the desired 96 Column MFCU channel number. Refer to I/O Base Section VI for typical system control numbers and an example for wiring the jumper chip.

DEVICE IDENTITY ADJUSTMENT

Jumper chip A3 of card 2 is wired to report the attached device capability. Table VI-1 shows which pins of the jumper chip should be connected for different ID's. Figure VI-1 shows an example of wiring in the read-punch-print ID.

Table VI-1

Capability	Connect	ID
Read-punch-print	PinA to PinP PinC to PinM	0001010
Multifunction	PinC to PinM	0001000
Punch	PinA to PinP	0000010
Read/Punch	PinA to PinP PinB to PinN	0000110
Read	PinA to PinP PinB to PinN PinD to PinL	0100110
Punch/Print	PinB to PinN PinD to PinL	0100100

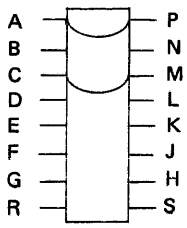


Fig. VI-1 CHIP A3 CARD 2 ID JUMPER CHIP EXAMPLE

Installation Procedures

PHYSICAL INSTALLATION

The 96 Column MFCU Control is installed in the I/O Base and cabled to the I/O Adapter Panel. The B9419 Interpreting Data Recorder (MFCU) is located to the right of the console and butted end to end with the table. With the corner table configuration the MFCU will be at right angles to the console and end to end with the table.

CARD LOADING

The 96 COL MFCU Control is contained on two cards. This control may be installed in either one of the two 2 card control slots. Refer to I/O Base Section VI for definition of these control slots.

PERIPHERAL TO I/O ADAPTER PANEL CABLING

The Interpreting Data Recorder has two data cables. One for the reader and one for the punch-printer. These two cables are identical. Connect the two card edge connectors to cards 14 and 15 of the top card rack in the Interpreting Data Recorder. Pin 1 is at the top of the card. Route the cables to the back of the Interpreting Data Recorder and out the bottom cable hole. Pass the cables under the unit to the trough at the table end. The cables are routed through the trough and straight up to the I/O Adapter Panel.

CONTROL TO I/O ADAPTER PANEL CABLING

Two identical Adapter cables are routed from frontplane connector #Y of Card 1 and Card 2 to the I/O Adapter Panel. Route Adapter cable from #Y Card 1 straight down to the trough at the bottom of the I/O Base. From the trough drop the cable straight down and into the table assembly. Route over and up to the I/O Adapter Panel. Mount the 50 pin receptacle on the I/O Adapter Panel. Connect the cable from the reader section of the Interpreting Data Recorder (cable from Card 14) to the receptacle and tighten. Route cable from card two in the same manner. Mount the receptacle on the I/O Adapter Panel. Connect the cable from the punch-printer section of the Interpreting Data Recorder to the receptacle and tighten. Run 1 foot 50 conductor ribbon cable from $Y card 1 to $Y card 2.

ELECTRICAL INSTALLATION

AC POWER

Route the Interpreting Data Recorder power cord alongside the previously laid data cables. Insert through trough at the end of the table and plug into a standard power receptacle on the AC Power Distribution Assembly.

PERIPHERAL/CONTROL CHECKOUT

Upon completion of the Interpreting Data Recorder installation run the 96 COL MFCU confidence routine and associated test routines to assure proper operation.